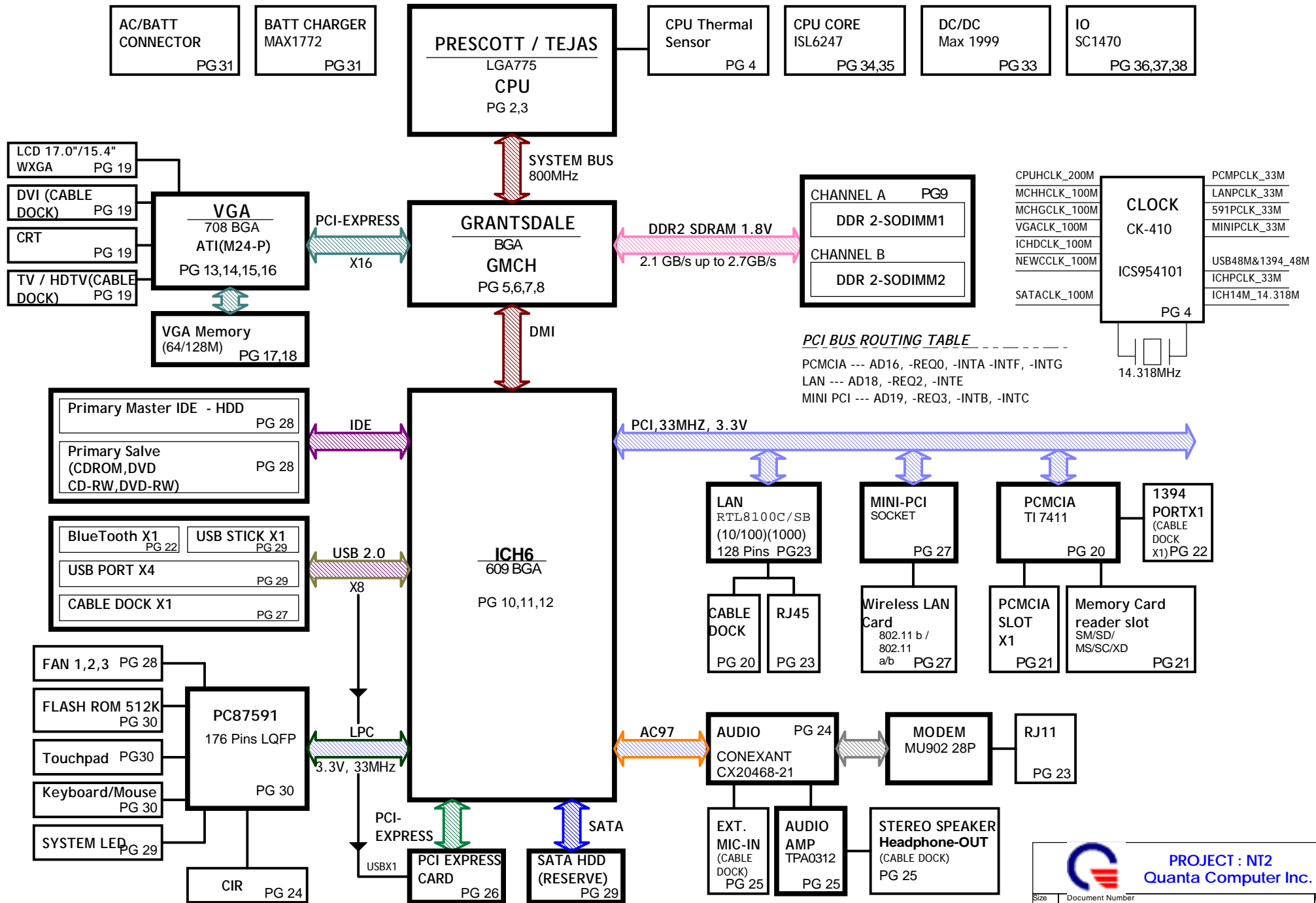
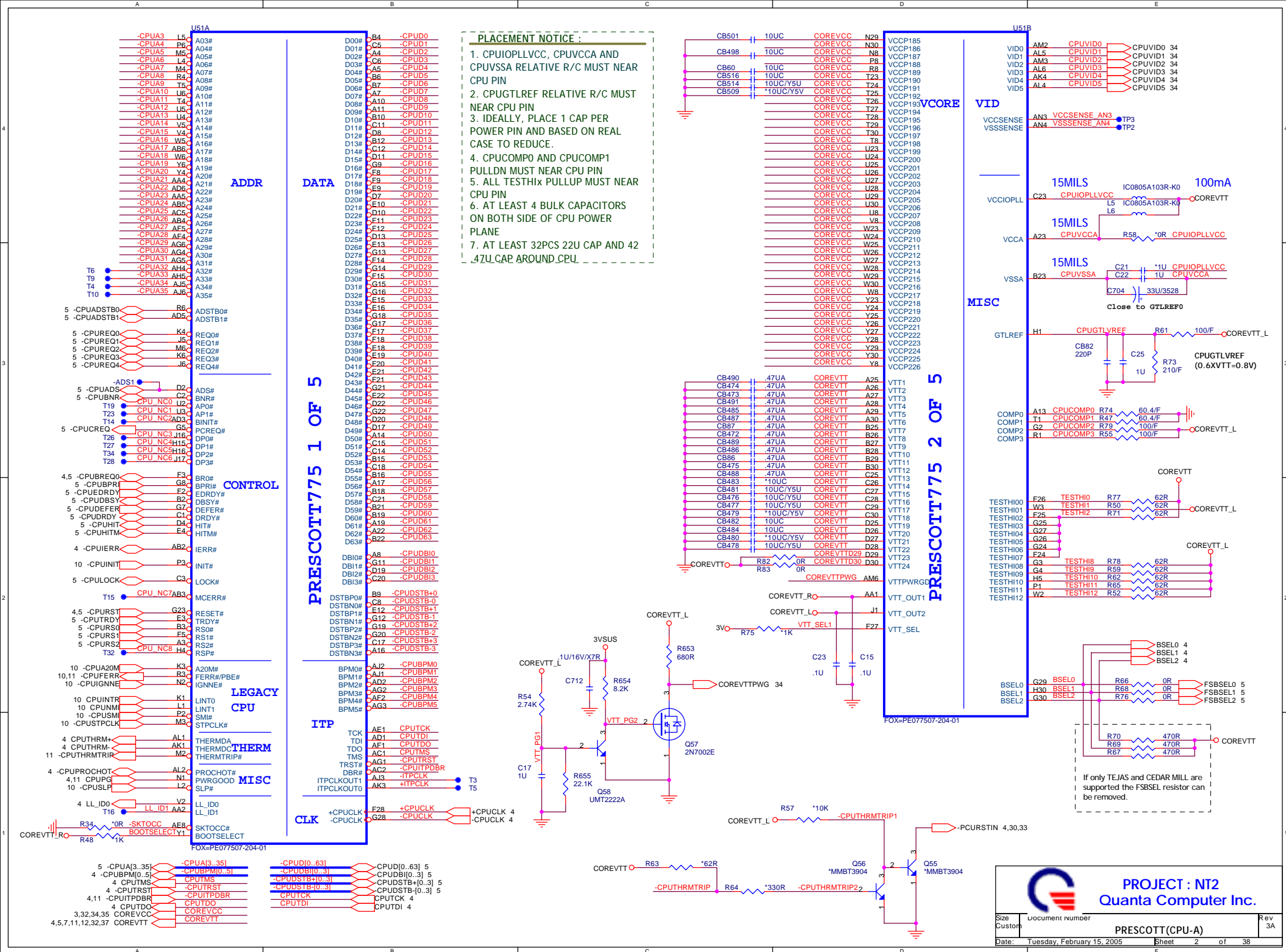
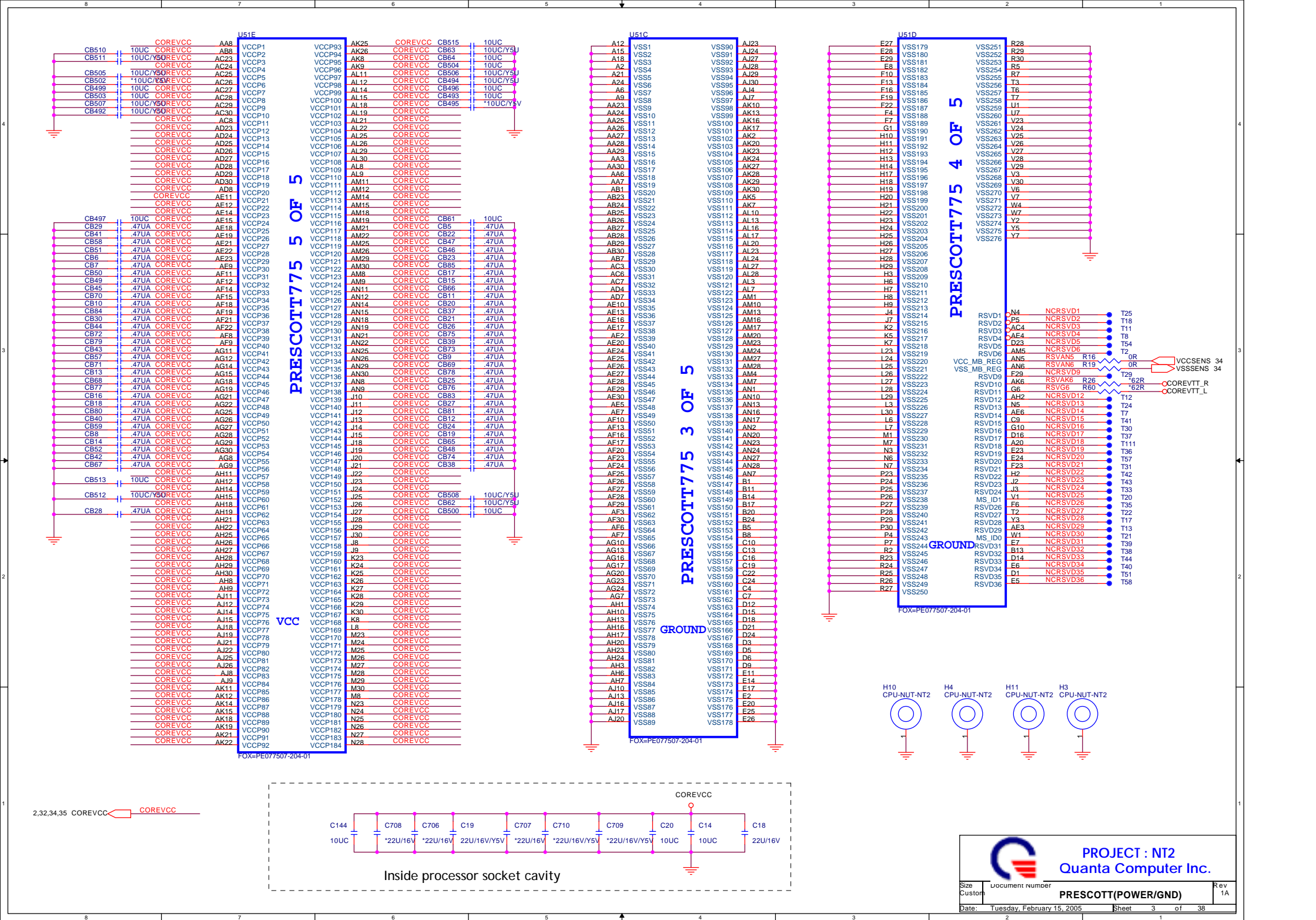
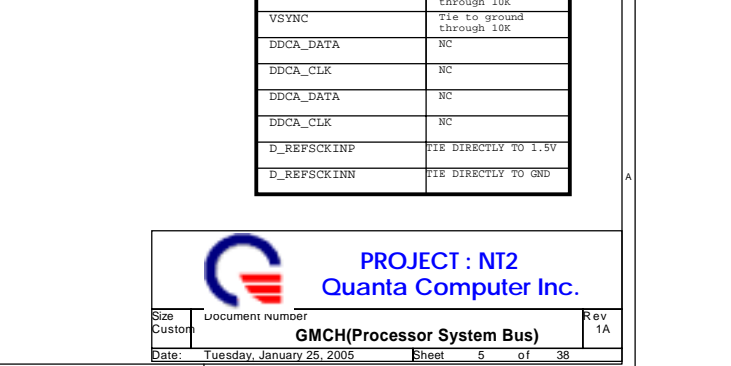
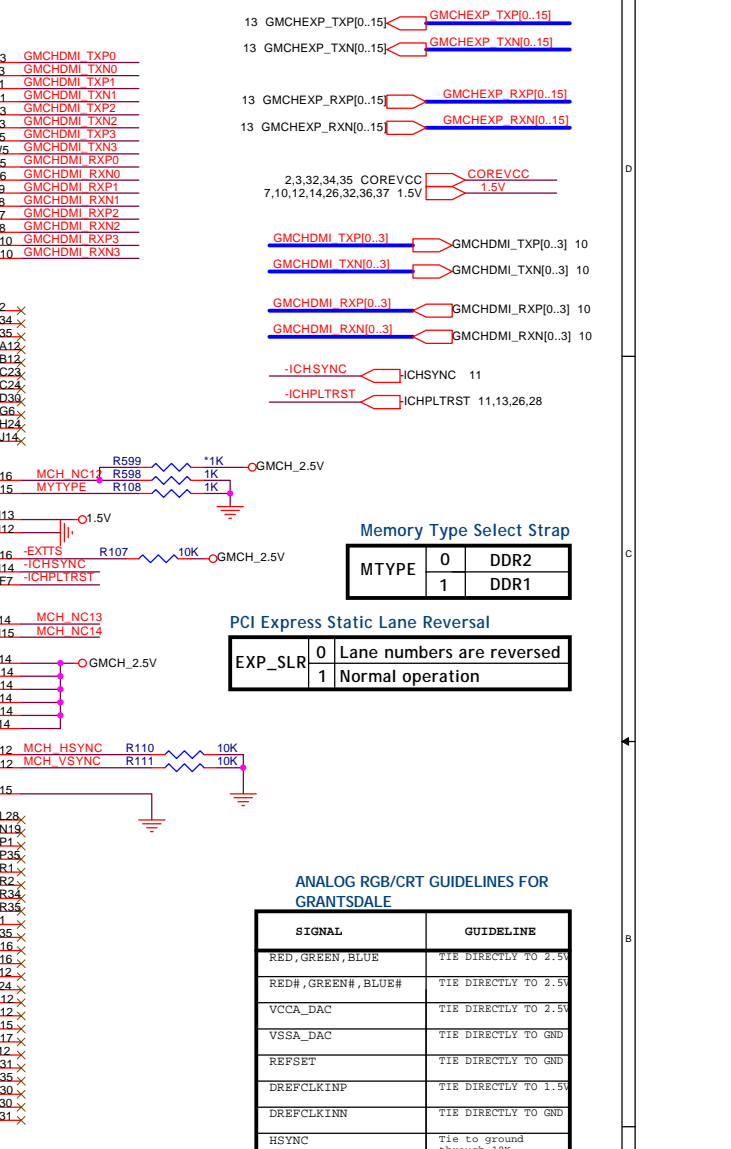
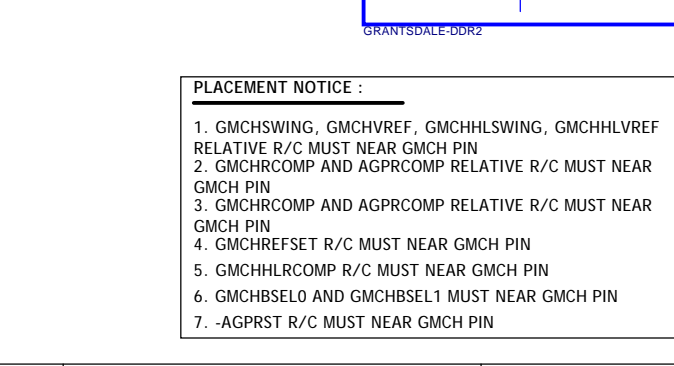
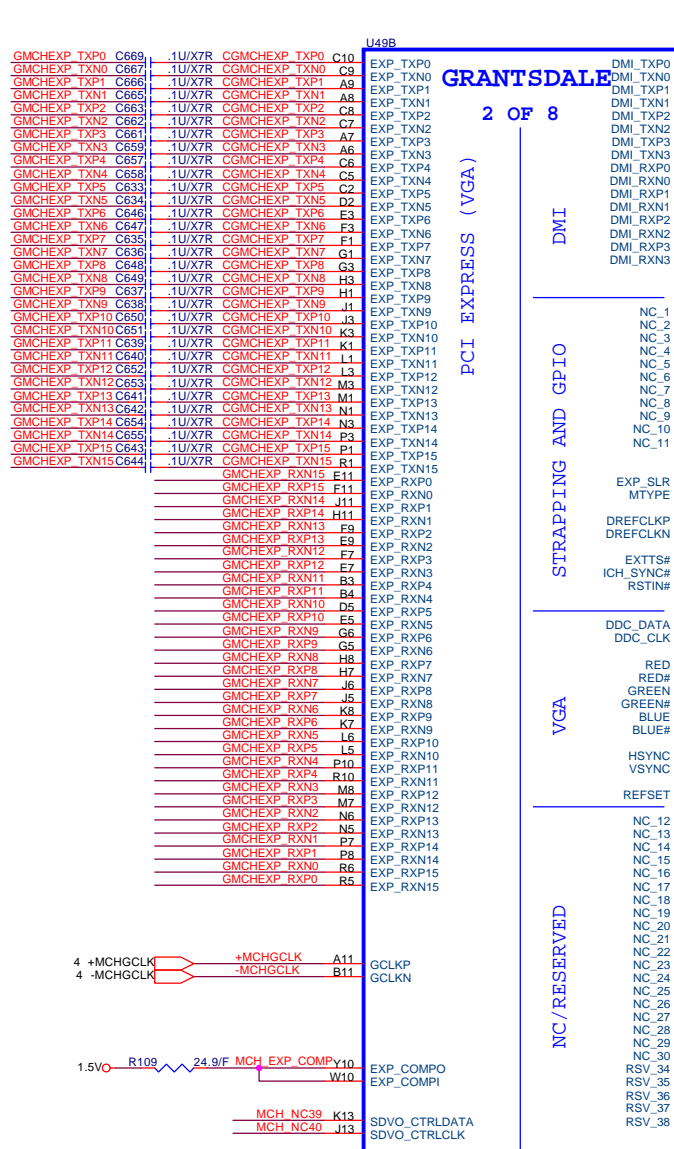
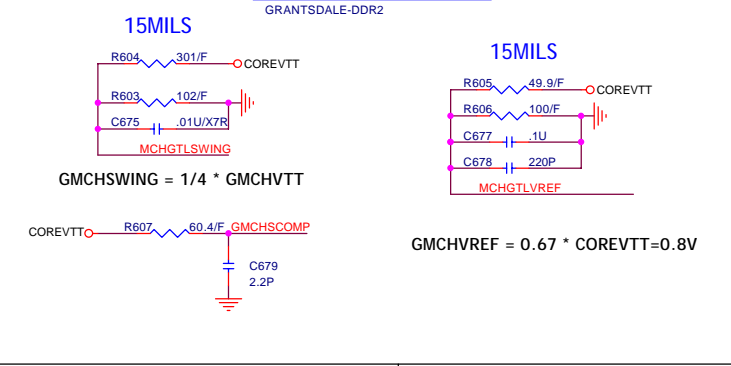
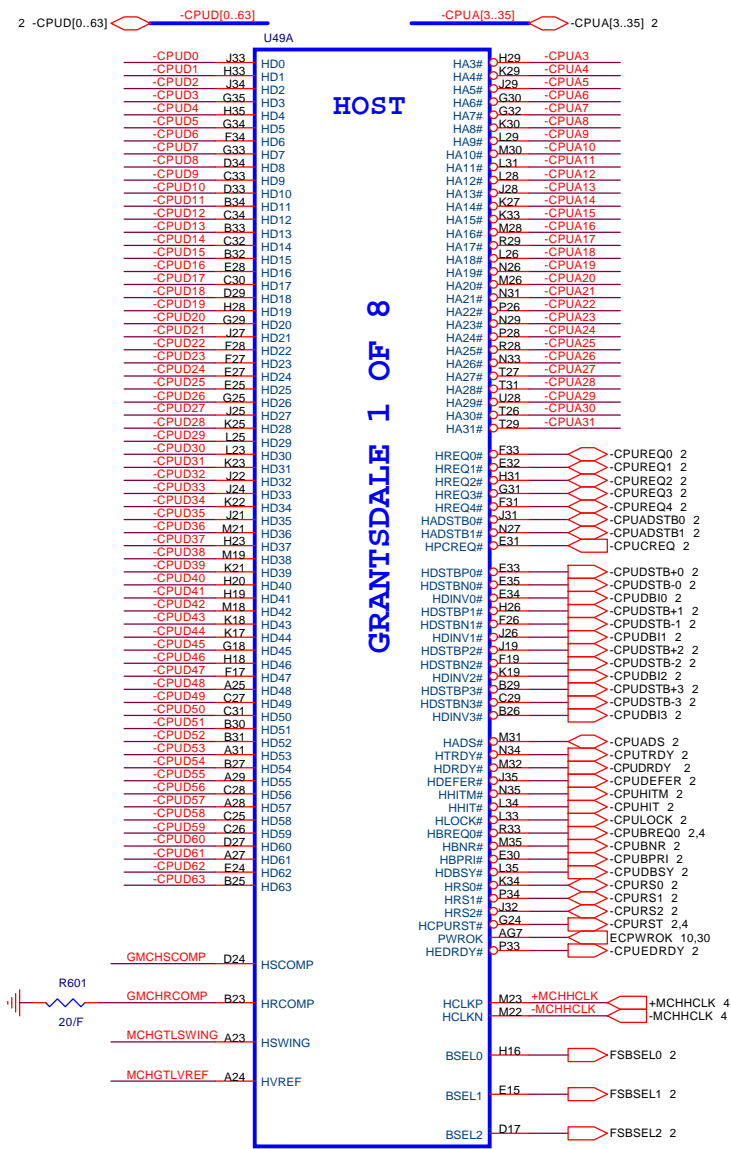


NT2 - Block Diagram

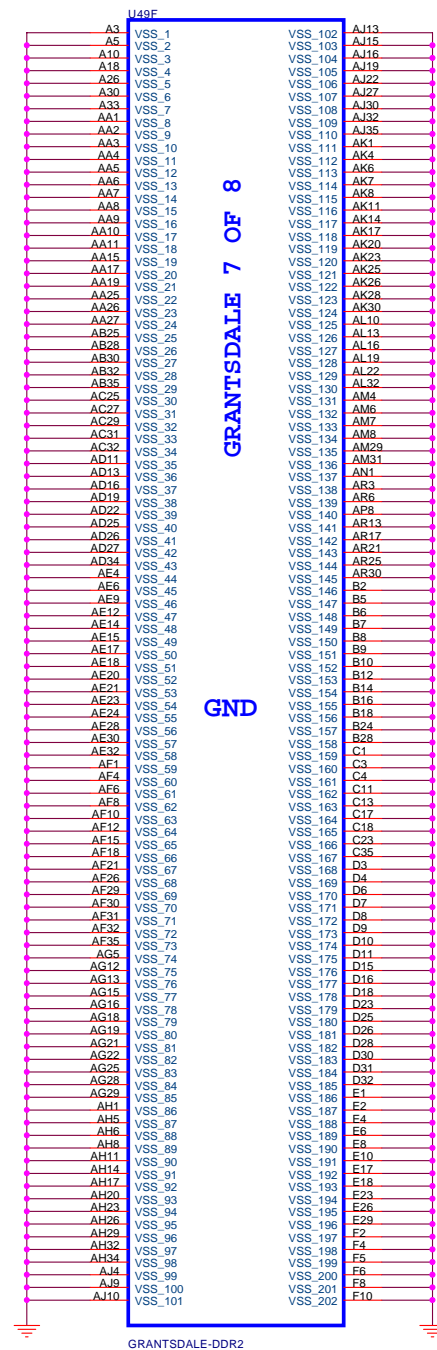
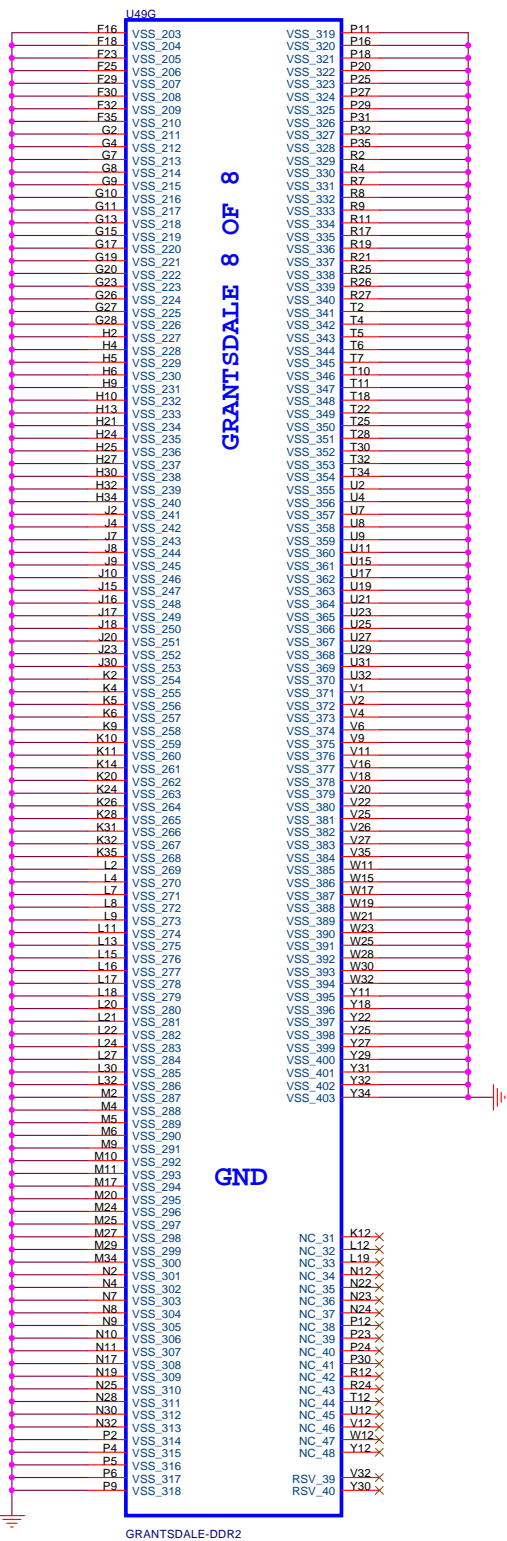


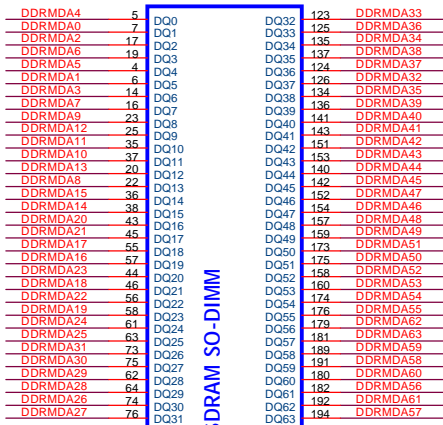






- PLACEMENT NOTICE :
1. GMCHSWING, GMCHVREF, GMCHHLSWING, GMCHHLVREF RELATIVE R/C MUST NEAR GMCH PIN
 2. GMCHRCOMP AND AGPRCOMP RELATIVE R/C MUST NEAR GMCH PIN
 3. GMCHRCOMP AND AGPRCOMP RELATIVE R/C MUST NEAR GMCH PIN
 4. GMCHREFSET R/C MUST NEAR GMCH PIN
 5. GMCHHLRCOMP R/C MUST NEAR GMCH PIN
 6. GMCHBSEL0 AND GMCHBSEL1 MUST NEAR GMCH PIN
 7. -AGPRST R/C MUST NEAR GMCH PIN

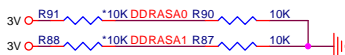




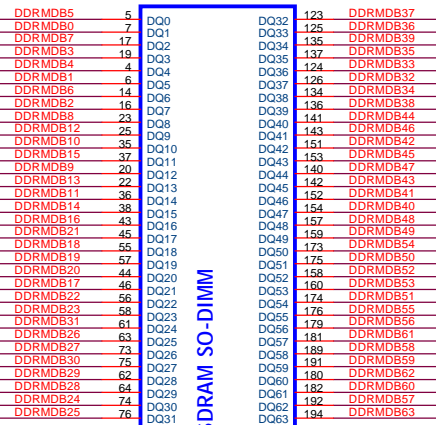
PC2100 DDR2 SDRAM SO-DIMM (200P)

CHANNEL A SINGLE DIMM

FOX=AS0A426-M2S-TR
CN29A



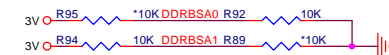
DIMM-1 Address 00



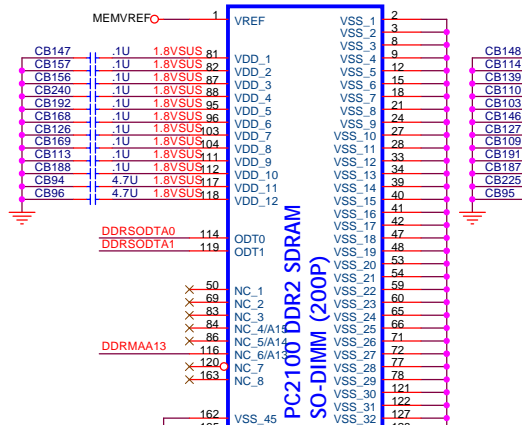
PC2100 DDR2 SDRAM SO-DIMM (200P)

CHANNEL B SINGLE DIMM

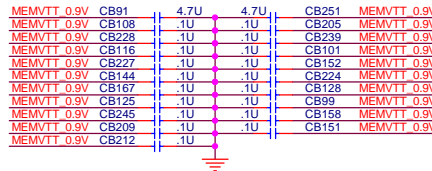
FOX=AS0A426-MAS-TR
CN28A



DIMM-2 Address 10

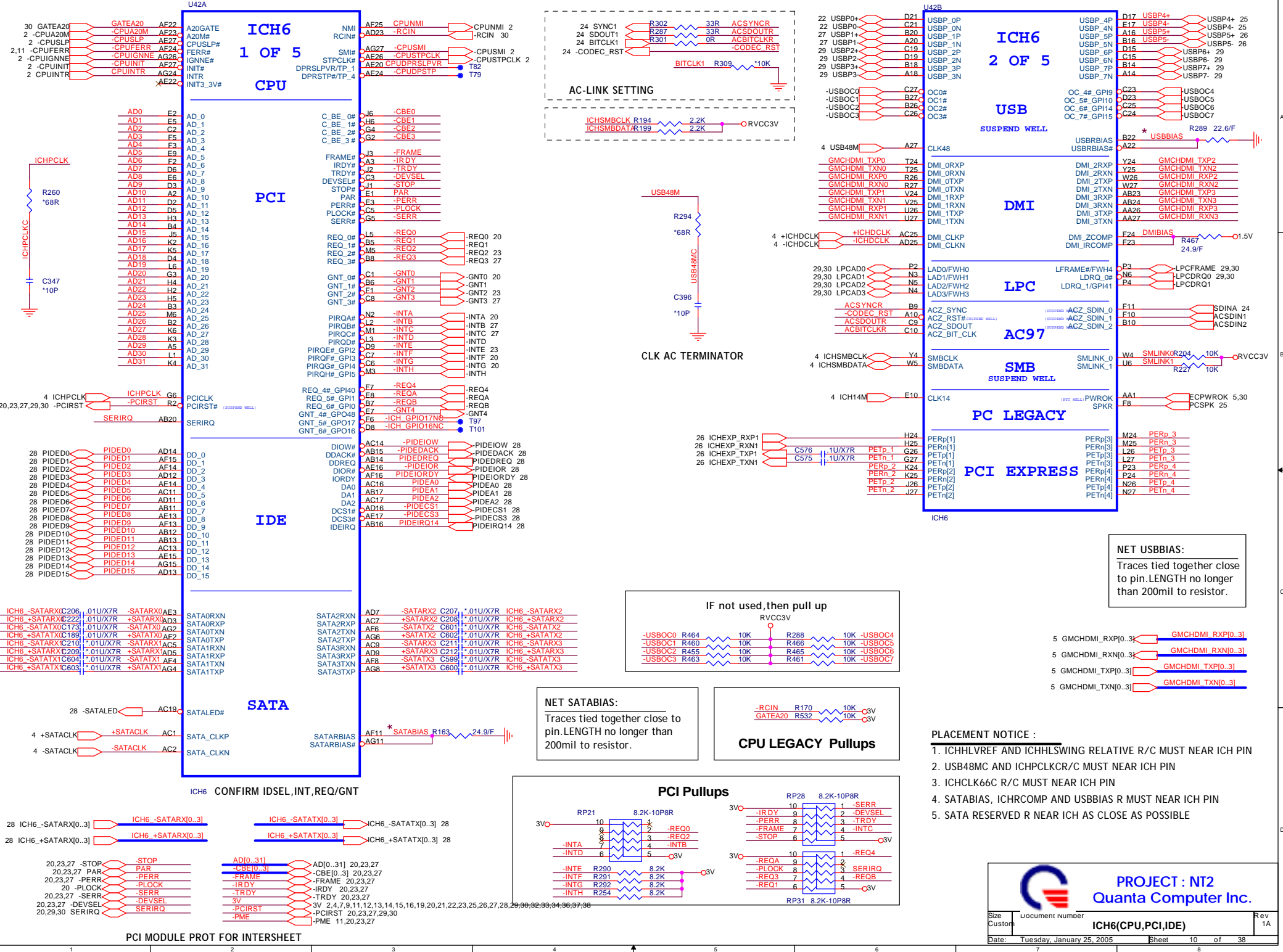


PC2100 DDR2 SDRAM SO-DIMM (200P)



- PLACEMENT NOTICE :
1. IDEALLY, PLACE 1 CAP PER POWER PIN AND BASED ON REAL CASE TO REDUCE.
 2. MEMVREF RELATIVE R/C IN MIDDLE OF TWO DIMM AND ONE CAP FOR EACH DIMM
 3. AT LEAST ONE CAP ON 1.275V FOR ONE TERMINATOR RESISTOR ARRAY
 4. TERMINATOR SIGNAL SHOULD BASED ON DIMM TO ARRANGE APPROPRIATE





GPIO PIN DEFINE

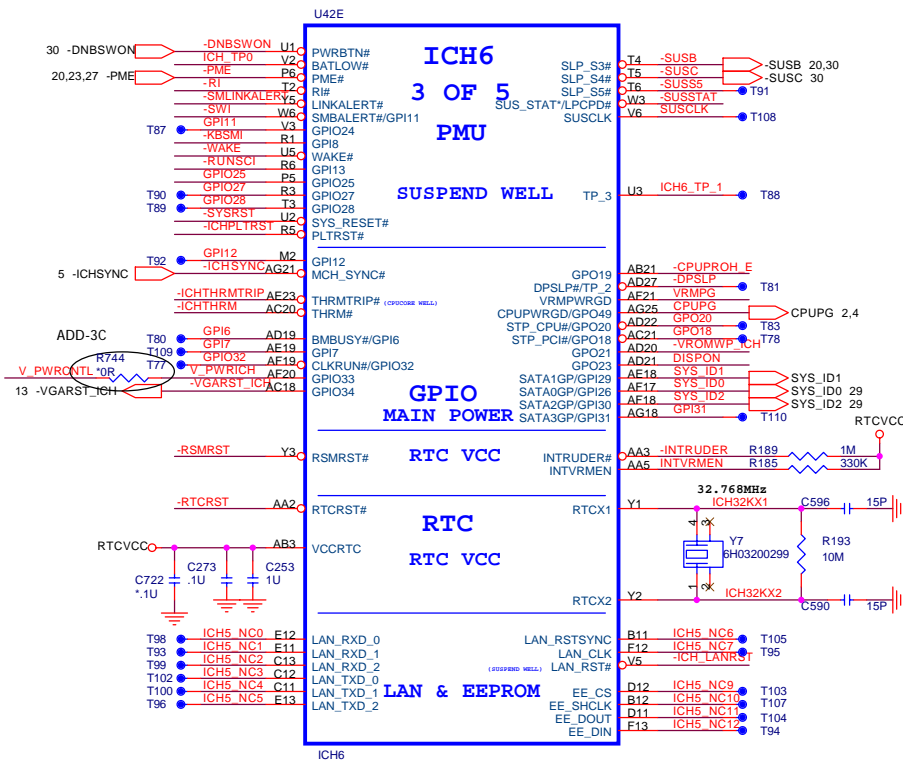
GPI6		PULL UP
GPI7	-KBSMI	PULL UP
GPI8	-SWI	PULL UP
GPI11		PULL UP
GPI12		PULL UP
GPI13	-RUNSCI	PULL UP
GPI26	SYS_ID0	PULL UP
GPI29	SYS_ID1	PULL UP
GPI30		PULL UP
GPI31		PULL UP
GPI18		SET OUTPUT
GPI19		SET OUTPUT
GPI20		SET OUTPUT
GPI21		SET OUTPUT
GPI23	DISPON	SET OUTPUT
GPI24		SET OUTPUT
GPI49	CPUPG	SET OUTPUT
GPI25		SET OUTPUT
GPI27		SET OUTPUT
GPI28		SET OUTPUT
GPI32		SET OUTPUT
GPI33		SET OUTPUT
GPI34		SET OUTPUT

Functional Straps

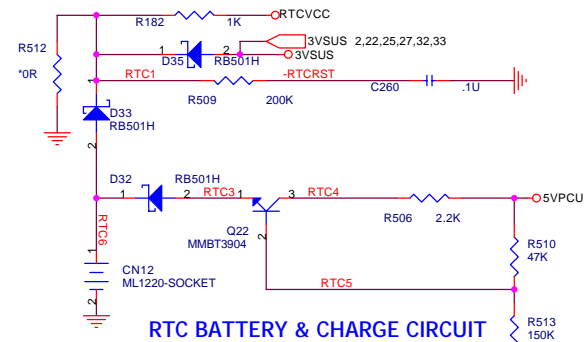
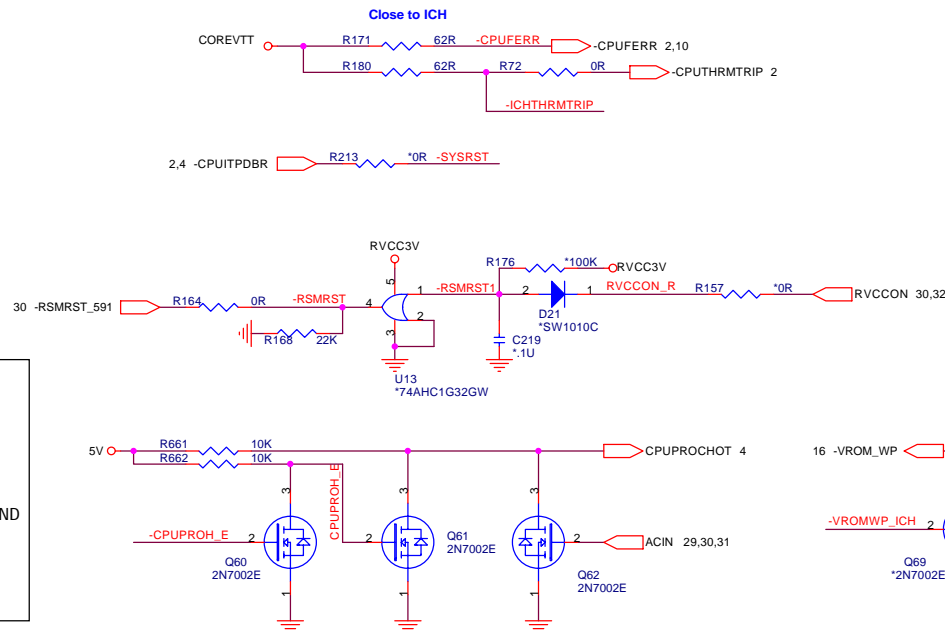
GNT[6]#/GPO[16]	Top-Block Swap Override Pull-Low : "top-block swap" mode
LINKALERT#	Reserved Requires an external pull-up resistor.
SPKR	No Reboot Pull-up : "No Reboot" mode
INTVRMEN	Integrated VccSus1.5 VRM enable/disable Pull-up : Enable integrated VccSus1.5V VRM
GPIO[25]	Integrated Vcc2.5 VRM enable/disable Pull-Low : Enable integrated Vcc2.5 VRM
EE_CS	Reserved Internal pull-down & should not be pull-high
GNT[5]#/GPO[17]	Boot BIOS Desination Selection This functionality for debug/testing only
EE_DOUT	Reserved Internal pull-up & should not be pull-low
ACZ_SDOUT	XOR chain Entrance / PCI Express port config bit1 Pull-low : allows entrance to XOR Chain testing
ACZ_SYNC	PCI Express Port Config bit 0 This signal has a weak internal pull-down
TP[1]	Internal pull-down & should not be pull-high
STATLED#	Internal pull-up & should not be pull-low
REQ[4:1]	XOR Chain Selection / See Chapter 8
TP[3]	XOR Chain Entrance / See Chapter 8 This signal should not be Pull-low unless using XOR Chain testing

DESIGN CHECK LIST :

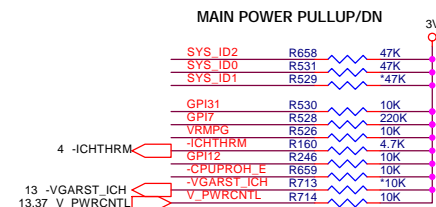
1. CLASSIFY THE POWER PLANE FOR PMU AND GPIO PIN
2. CLASSIFY GPI AND GPO PIN
3. COMMON PIN FOR PMU INPUT: -PME, BATLOW, -RI, -WAKESCI, RUNSCI, KBSMI AND -DNBSWON
4. USUALLY USED GPIO PIN : DISPON, CRTSENSE, SPKOFF
5. USUALLY USED CLK CONTRL PIN : -CPUSTP, -PCISTP, -SUSA AND -SUSSTAT
6. AGP PMU PIN : -AGPBUSY AND -STPAGP
7. CHECK -PCIRST BUFFERAND PWROK SIGNAL
8. CHECK -RSMRST CIRCUI



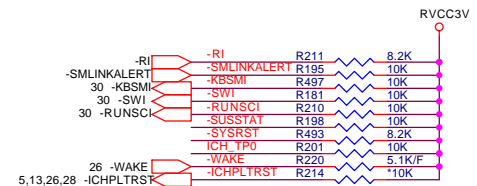
ASSUME S5 SUPPORT



RTC BATTERY & CHARGE CIRCUIT



SUSPEND WELL PULLUP



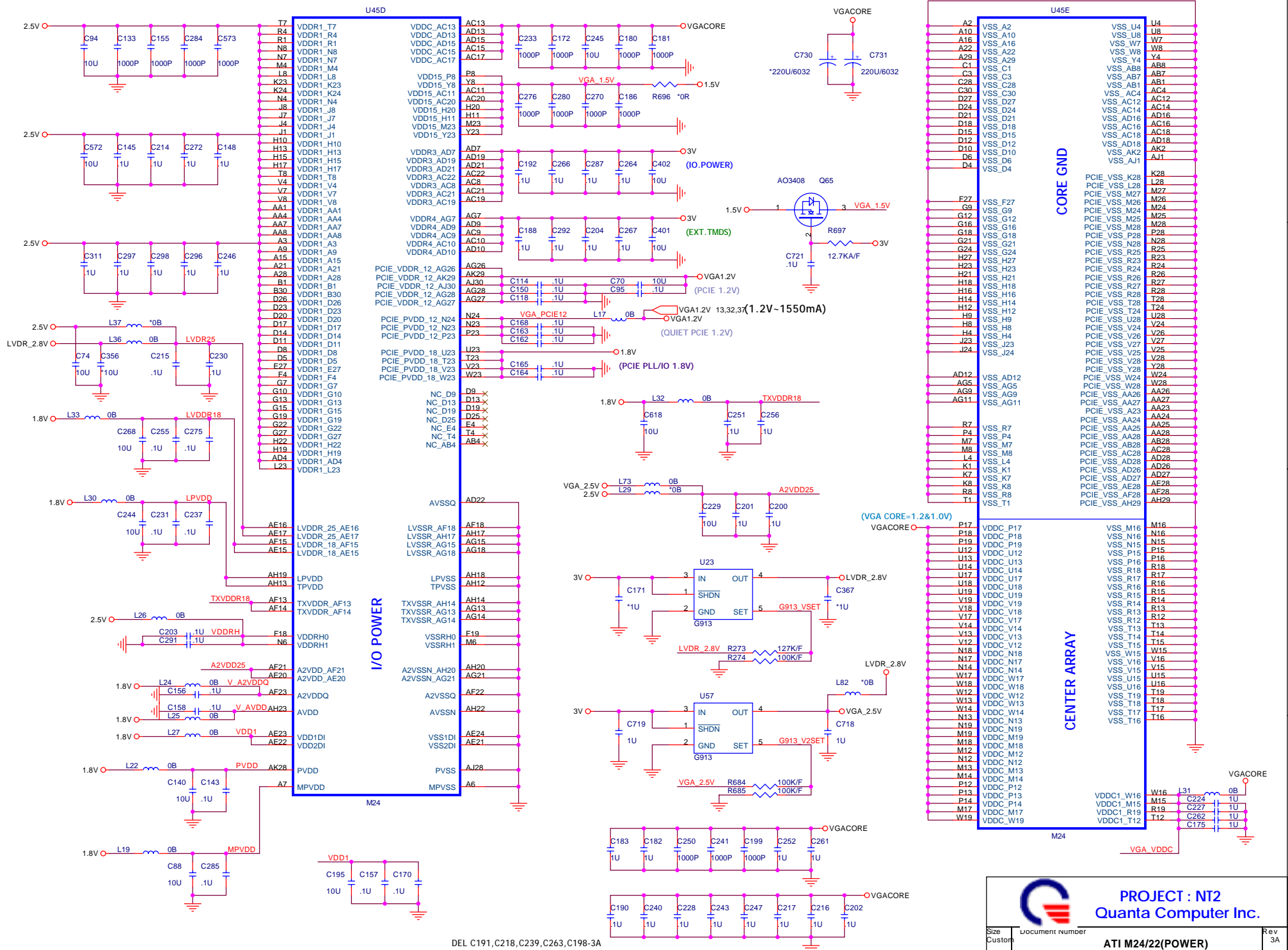
PLACEMENT NOTICE :

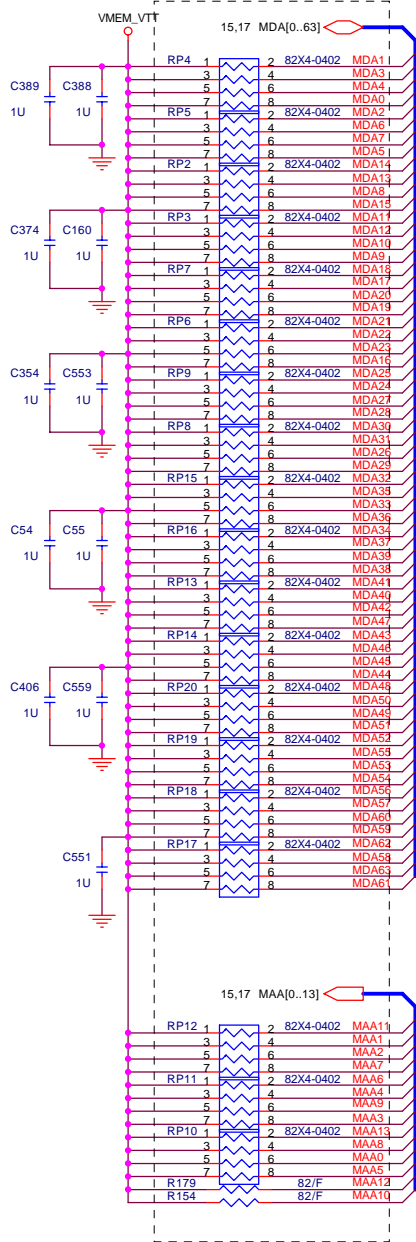
1. ONE BYPASS CAP FOR EACH ICH PIN IF POSSIBLE
2. RTC XTAL MUST NEAR ICH
3. PUT RTC BAT CIRCUIT AS A GROUP
4. REF5VSUS AND REF5V R/C/D NEAR ICH PIN



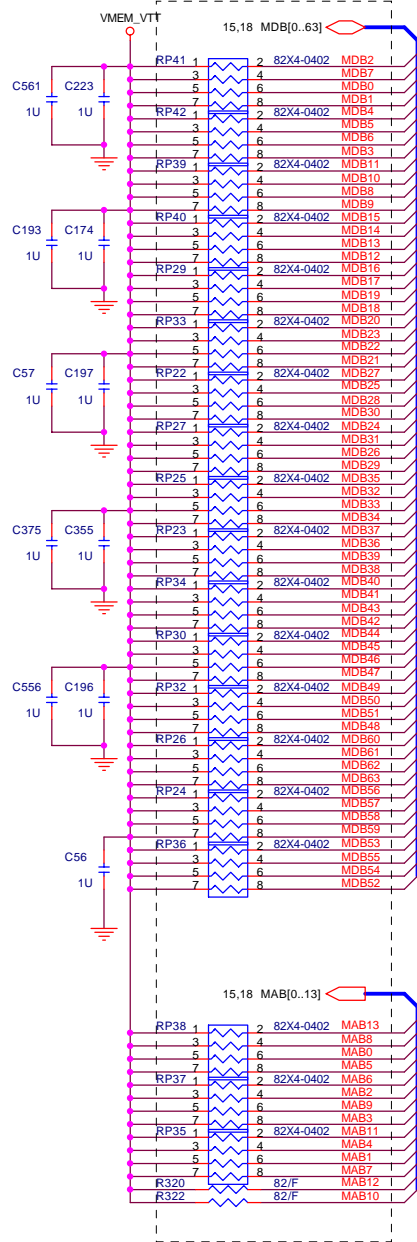
PROJECT : NT2
Quanta Computer Inc.

Size	Document number	Rev
Custom	ICH6(GPIO/MISC)	3C
Date:	Wednesday, January 26, 2005	Sheet 11 of 38

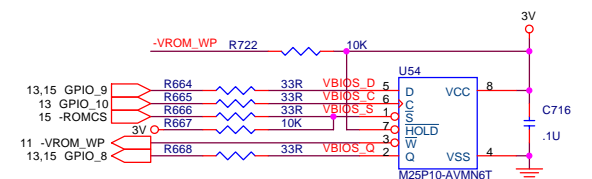
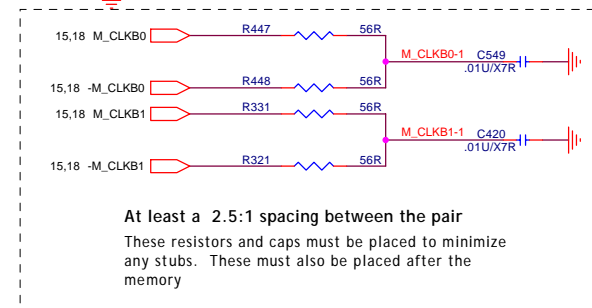
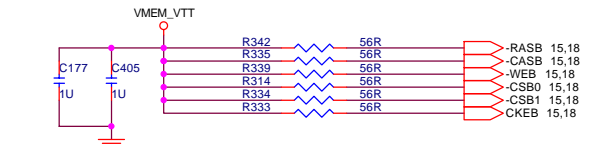
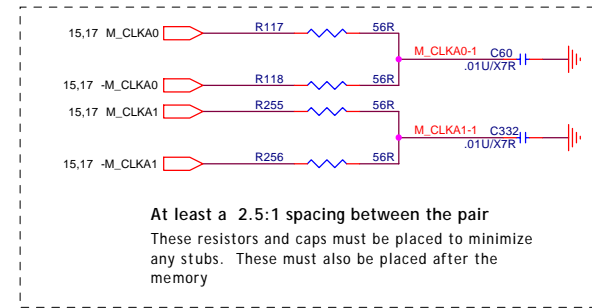
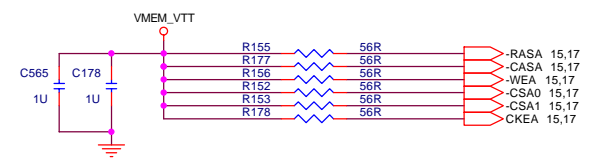
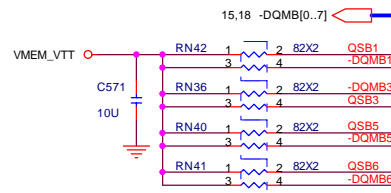
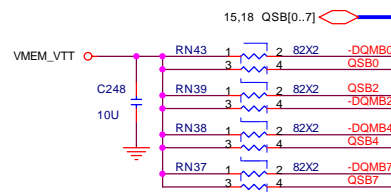
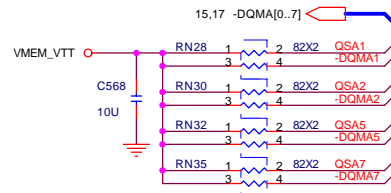
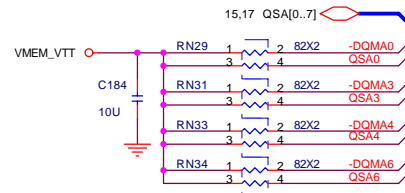




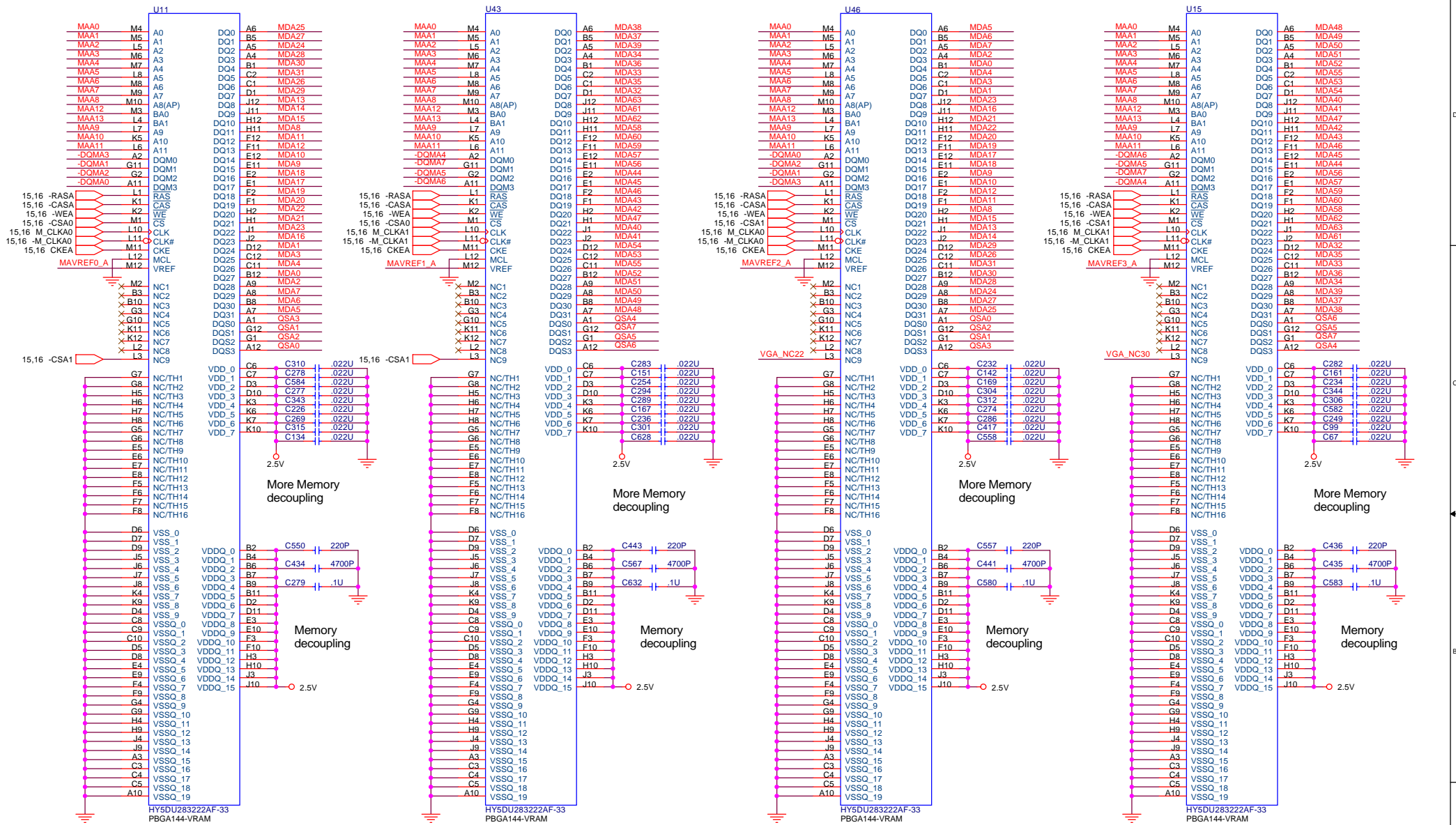
Place at nets mid point



Place at nets mid point




SERIAL ROM



VGA DDR MEMORY A

@64/128MBytes DDR 128Mbit 1MX32X4 uBGA

- MAA[0..13] 15,16
- MDA[0..63] 15,16
- DQMA[0..7] 15,16
- QSA[0..7] 15,16



PROJECT : NT2
Quanta Computer Inc.

Size Custom

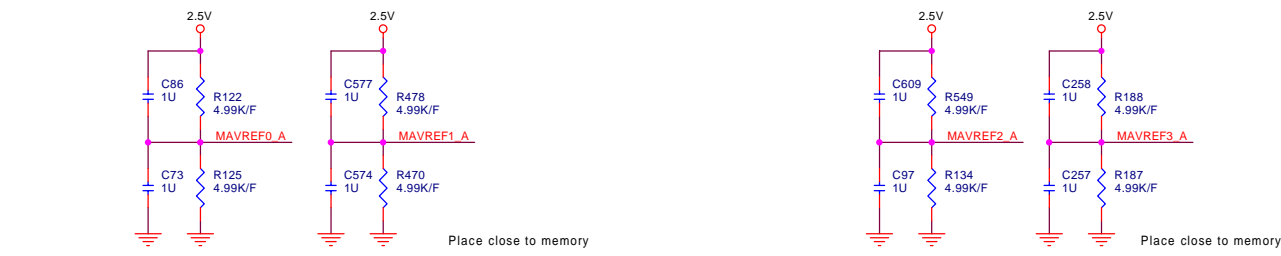
Document number

VGA DDR VRAM-A CANNEL

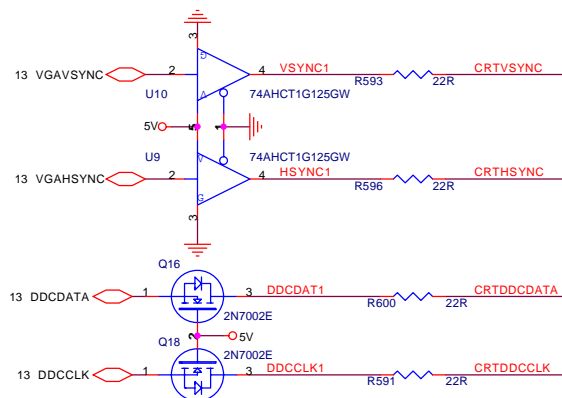
Date: Tuesday, January 25, 2005

Sheet 17 of 38

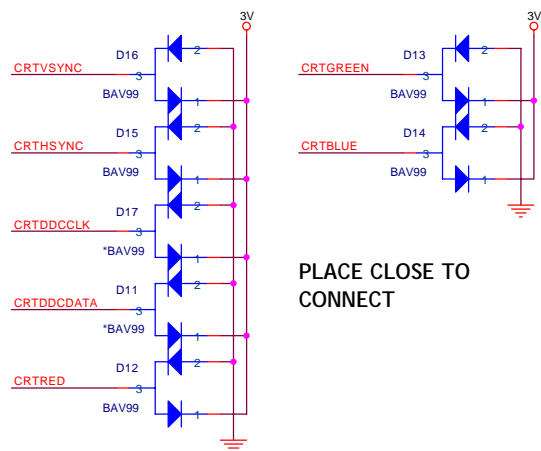
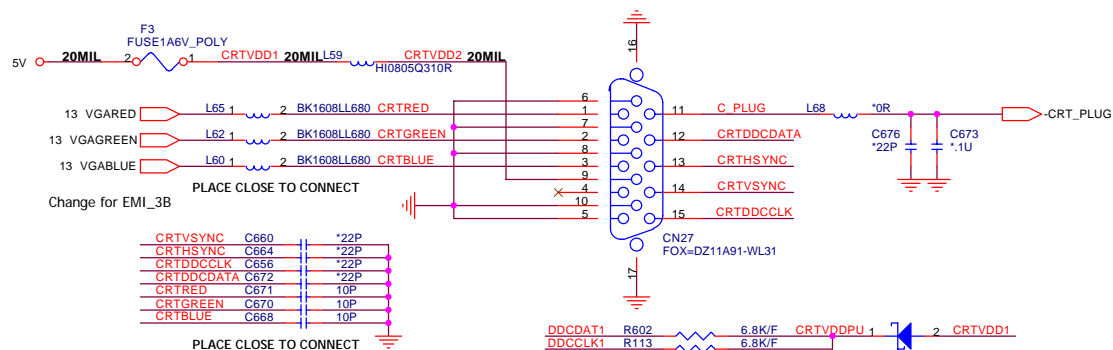
Rev 1A



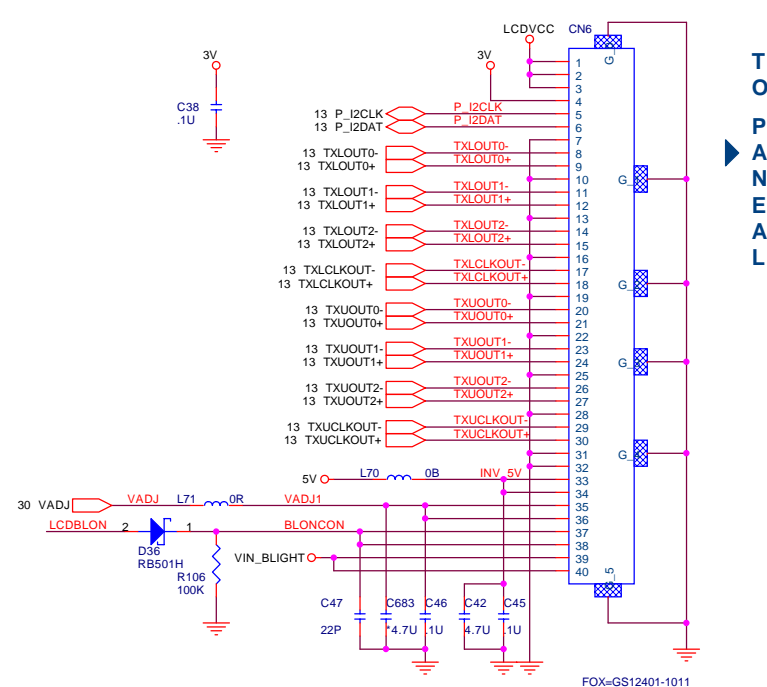




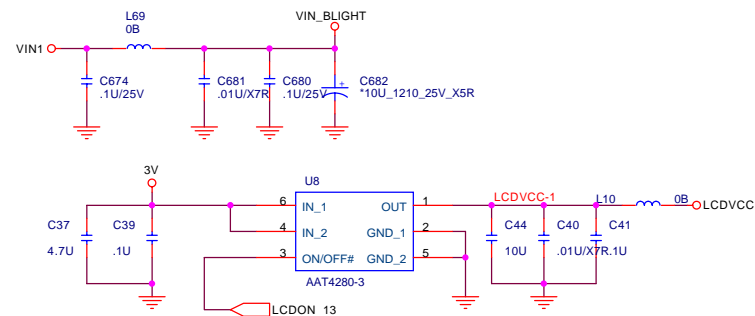
CRT PORT



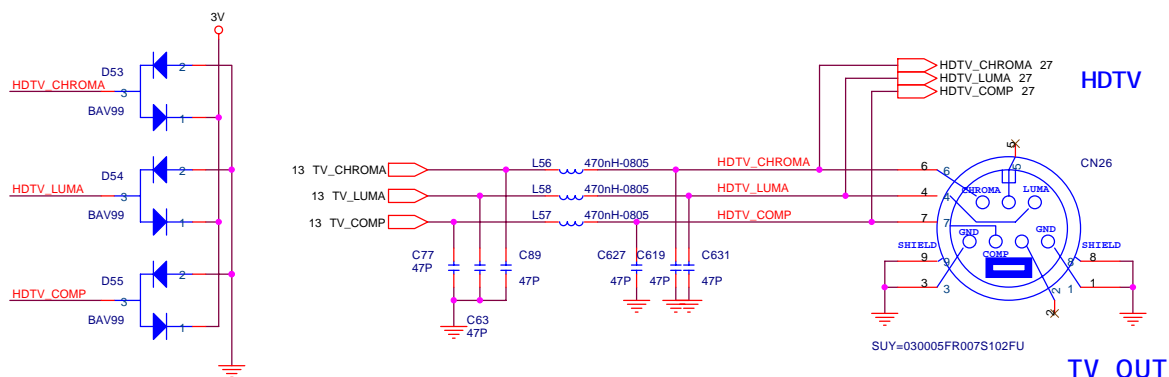
PLACE CLOSE TO CONNECT



TO PANEL

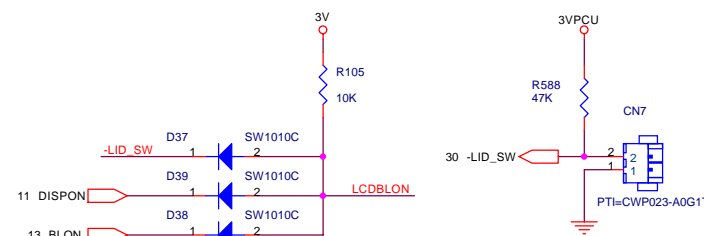


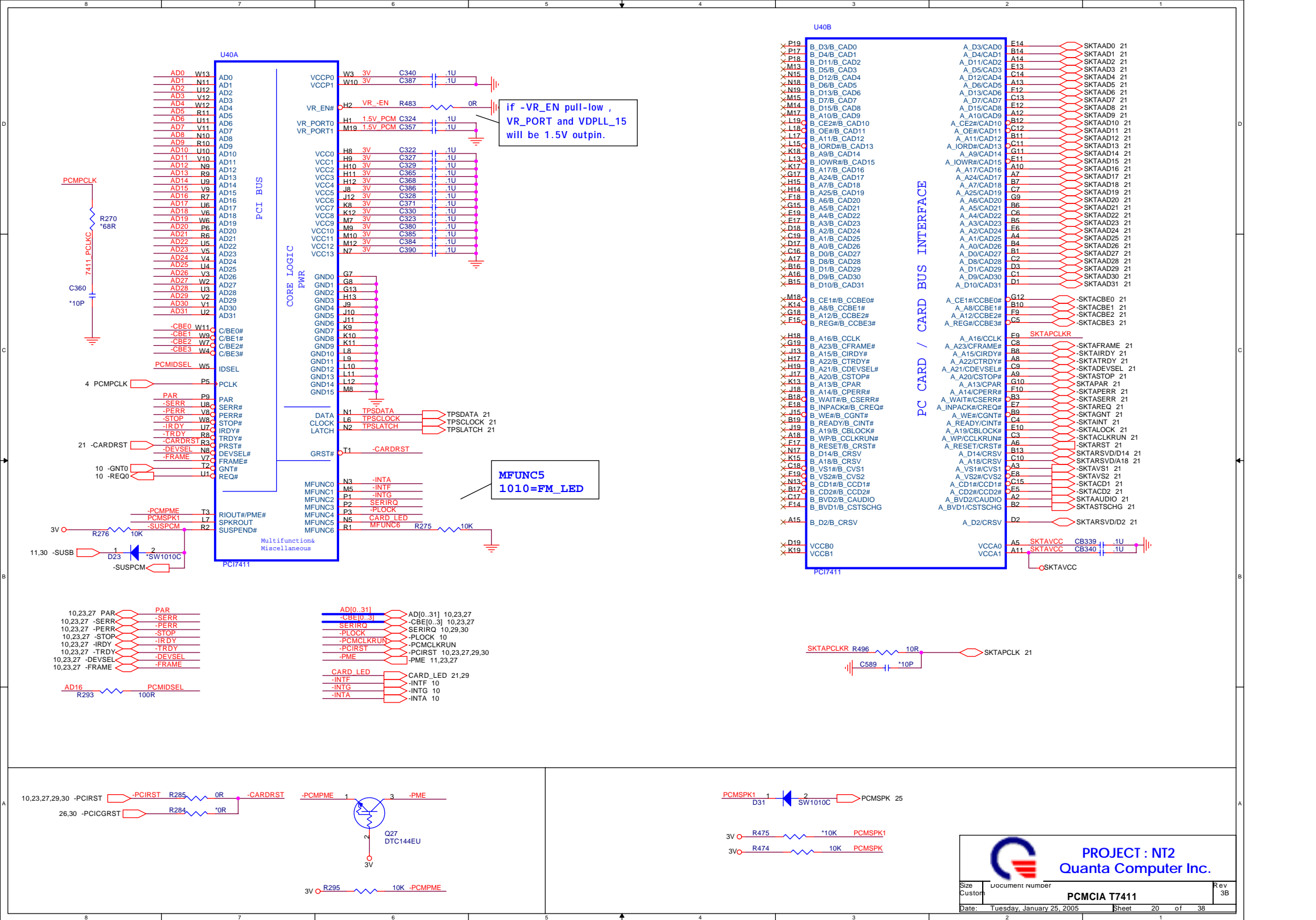
BACKLIGHT CONTROL

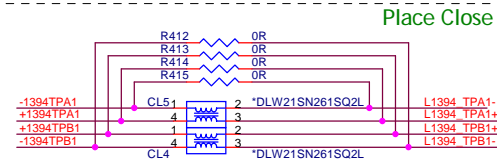
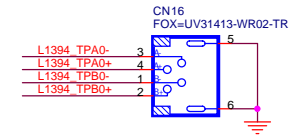
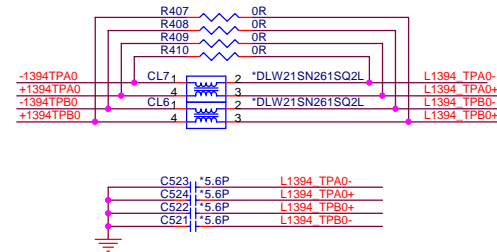
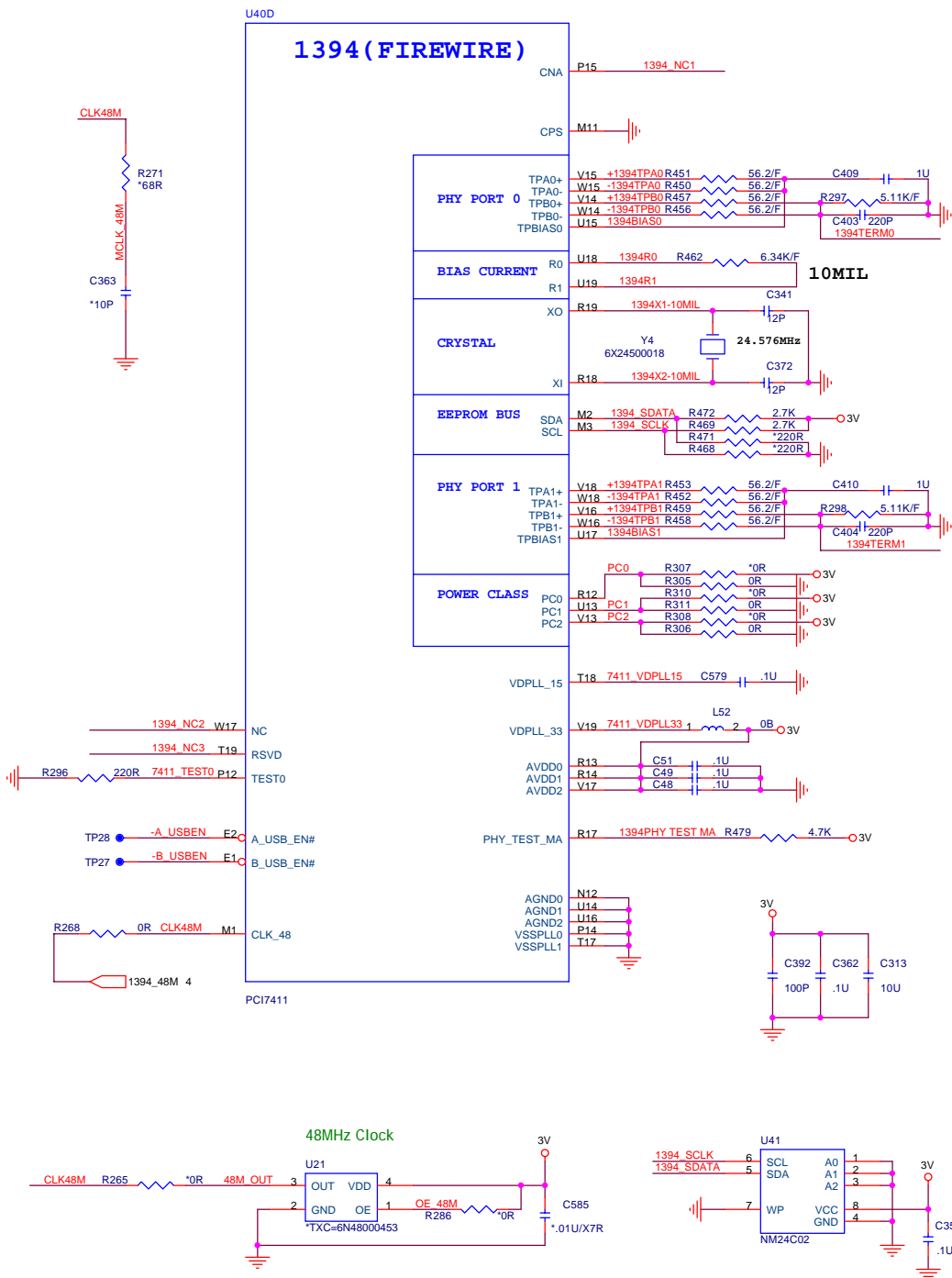


HDTV

TV_OUT





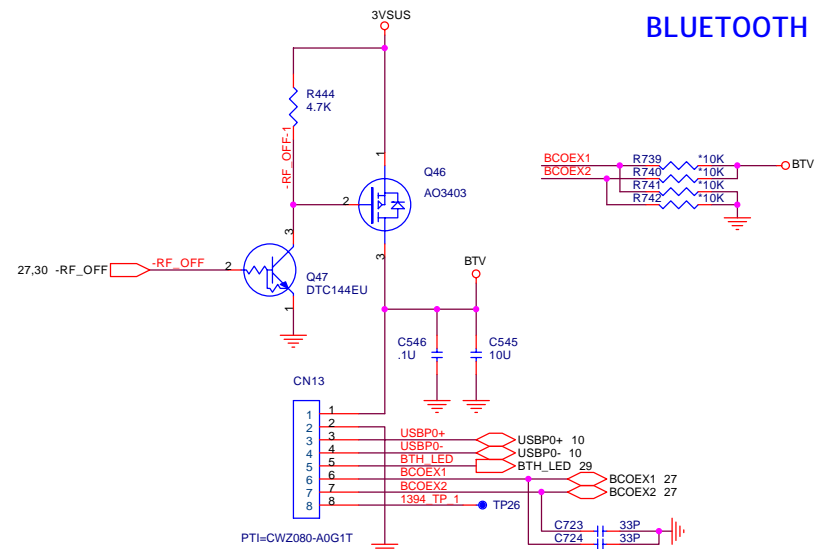


Place Close to DOCK CON.

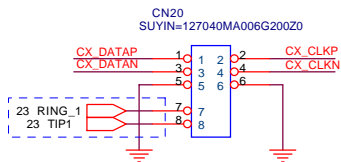
NOTE:

- All 1394 signals must be routed on top side only
- 110 ohm +- 5% differential pairs must be used
- Differential pairs must be 5 mills wide and 10 mills apart
- Parallelism must be maintained throughout differential pairs
- Minimum rise time @ 500 ps

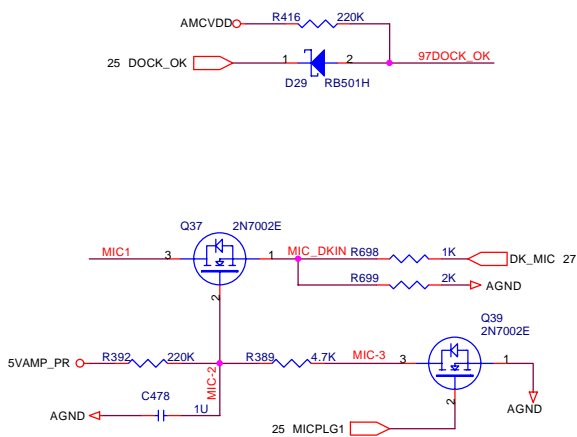
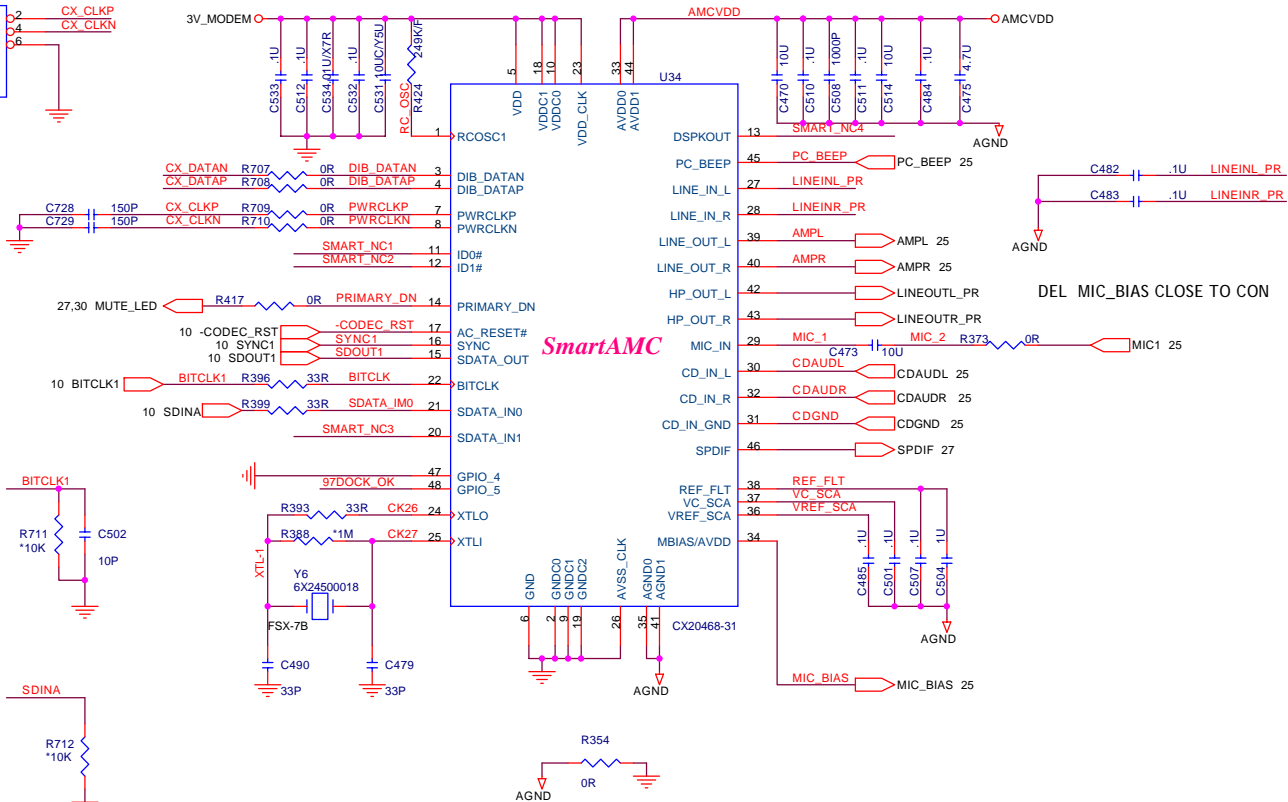
- Fbw @ 700 MHz
- Lambda/2 = 3 inches
- Differential pair must be routed with equal lengths no longer than 3 inches
- Stubs must be kept as short as possible
- All components must be place as close to device as possible



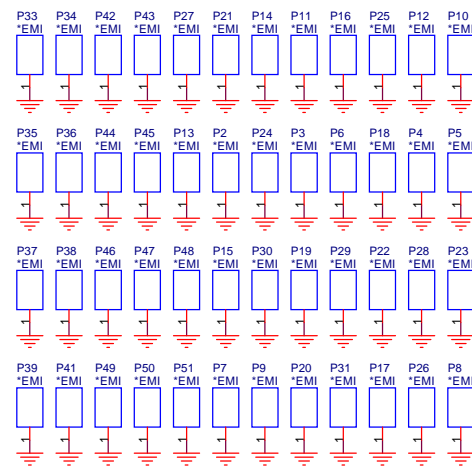
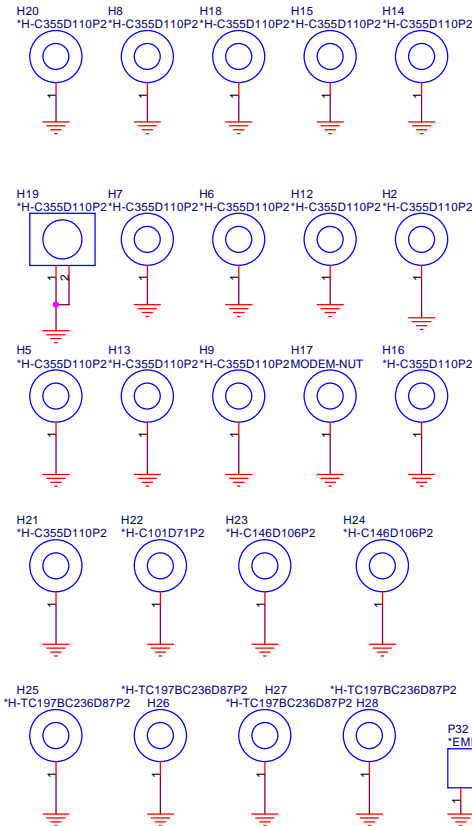
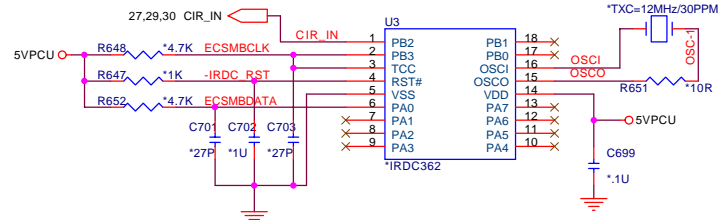
PROJECT : NT2
Quanta Computer Inc.



Keep away 3mm
with other signal

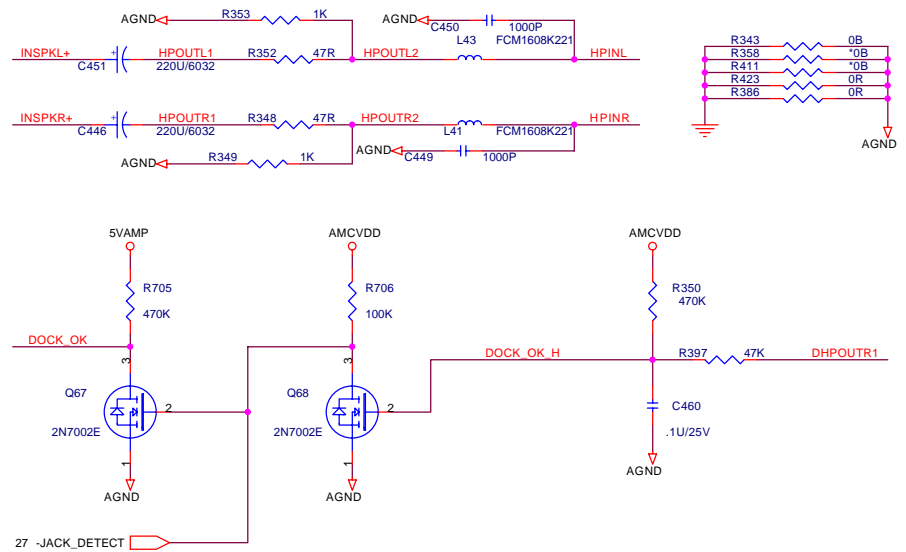
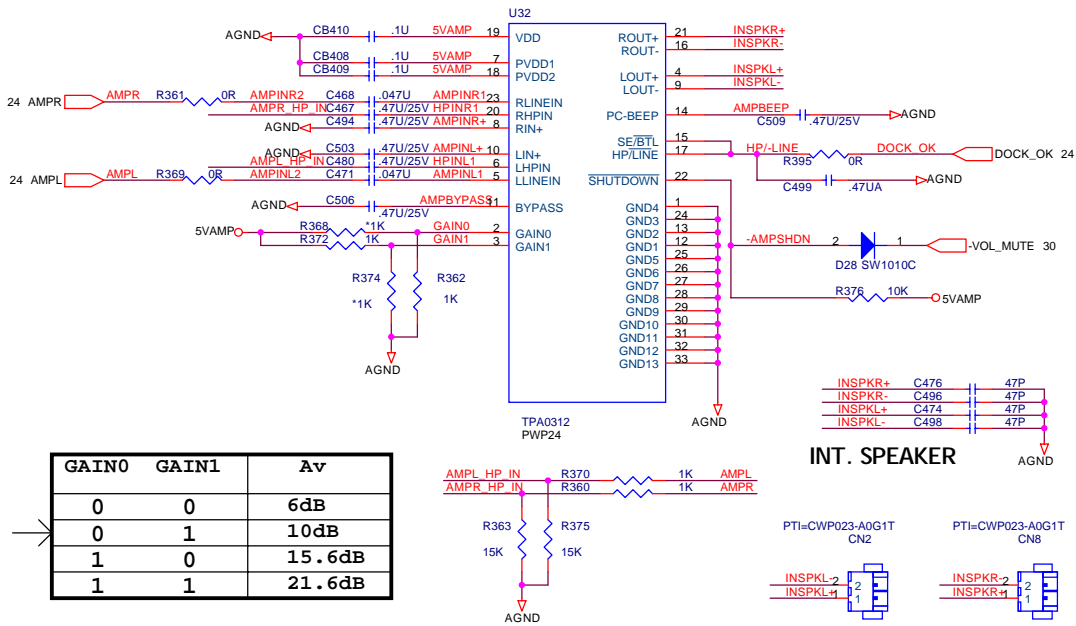


4.13.30 ECSMBDATA
4.13.30 ECSMBCLK

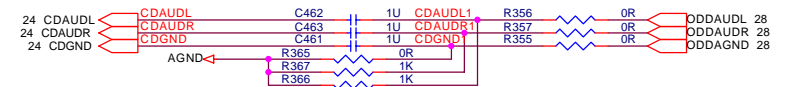


PROJECT : NT2
Quanta Computer Inc.

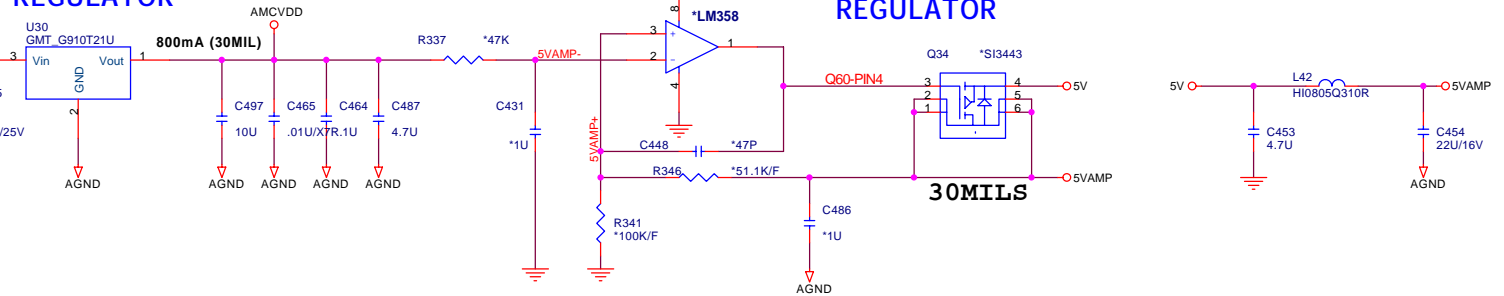
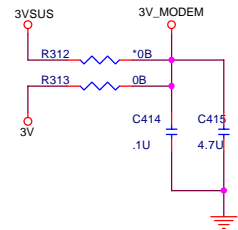
AUDIO AMPLIFIER



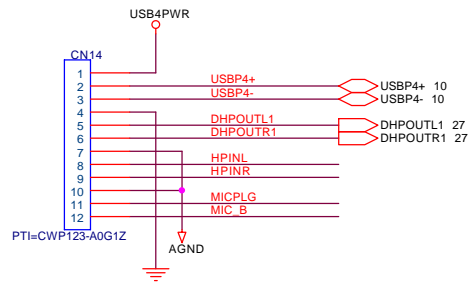
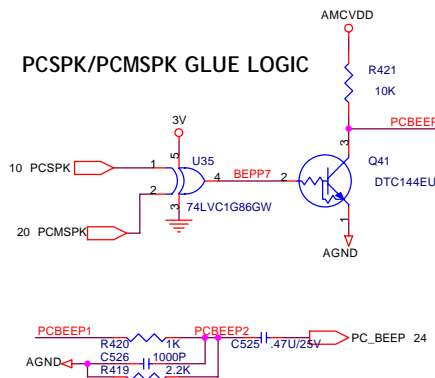
CD/PHONE INPUT & MONOOUT



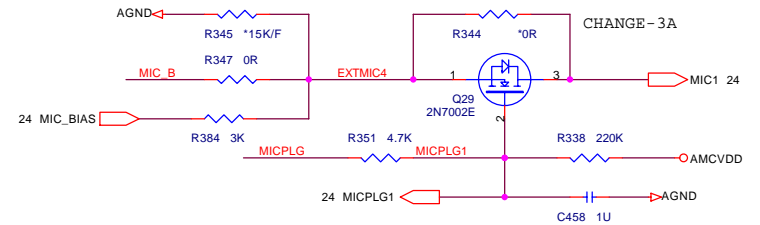
3VAUD REGULATOR



PCSPK/PCMSPK GLUE LOGIC

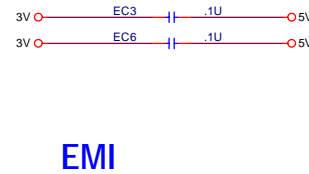
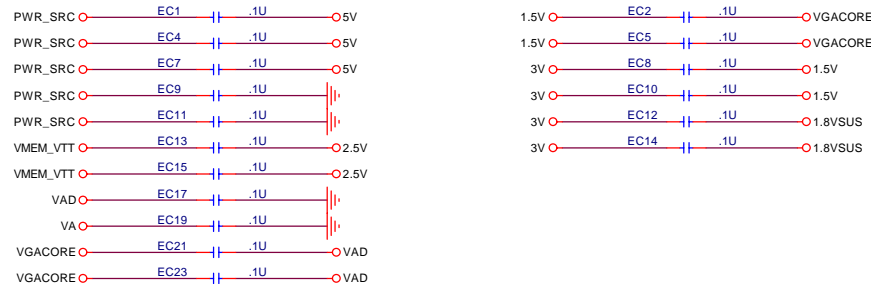
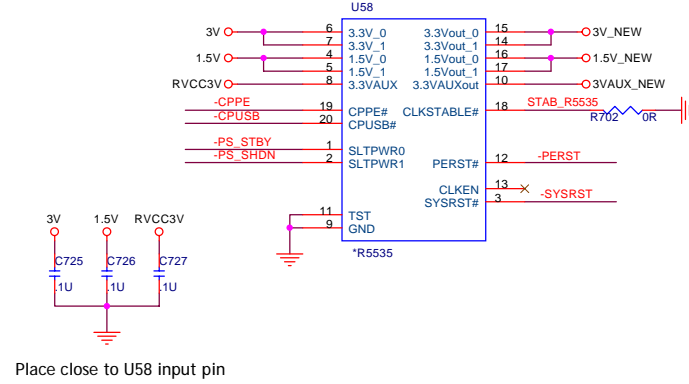
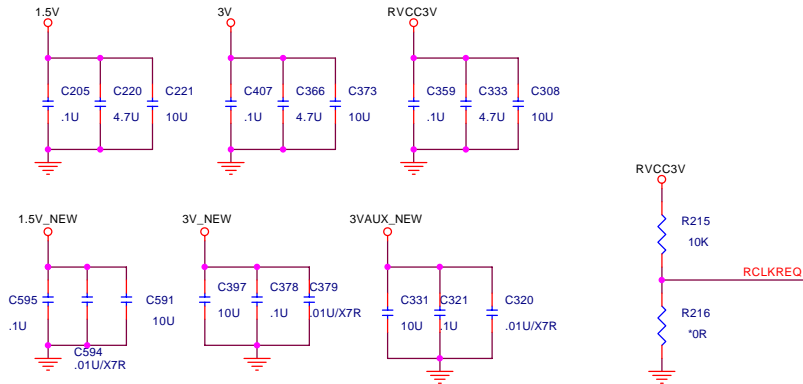
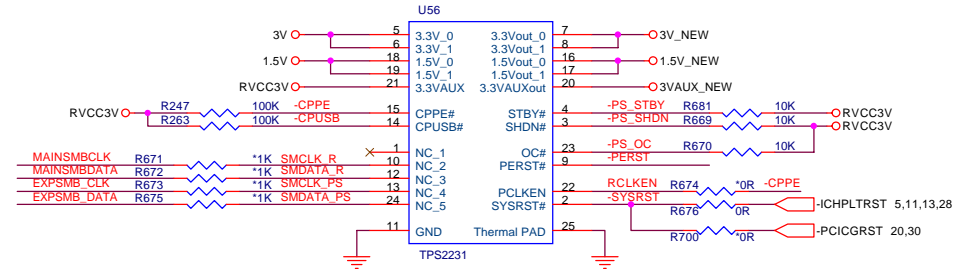
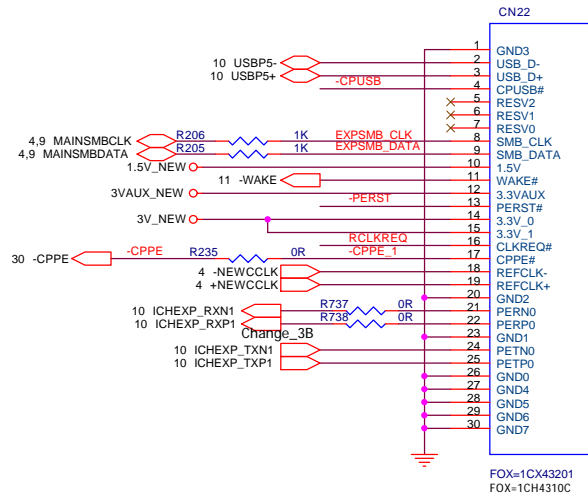


EXT MIC



PROJECT : NT2
Quanta Computer Inc.

Size Custom	Document number AUDIO AMP, HEADPHONE&SPEAKER	Rev 3B
Date: Tuesday, February 15, 2005	Sheet 25 of 38	



EMI

96	AD0	Mini PCI
99	AD1	
94	AD2	
95	AD3	Type III
92	AD4	
91	AD5	
90		

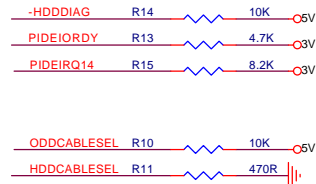
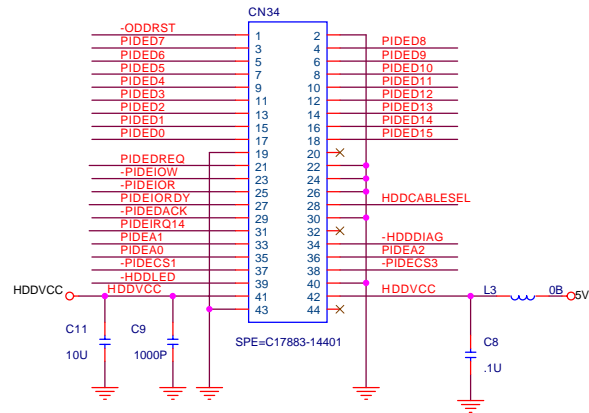


PROJECT : NT2
Quanta Computer Inc.

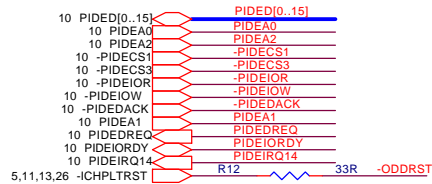
MINI PCI & DOKING

Size Custom	Document number	Rev 3B
MINI PCI & DOKING		
Date: Tuesday, January 25, 2005	Sheet 27 of 38	

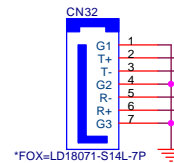
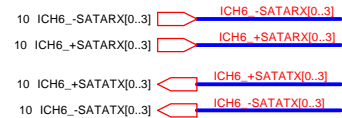
HDD CONNECTOR



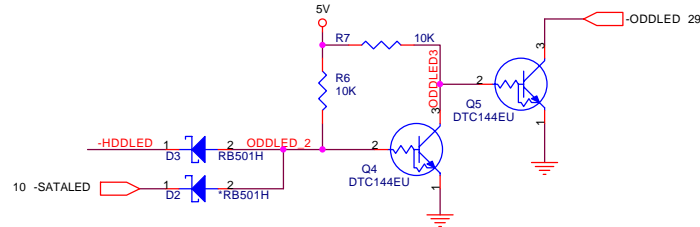
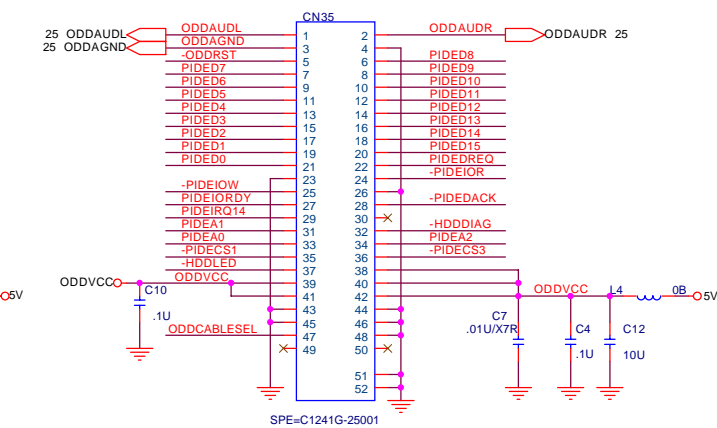
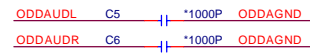
CABLESEL: H=SLAVE L=MASTER



SATA HDD CONNECTOR

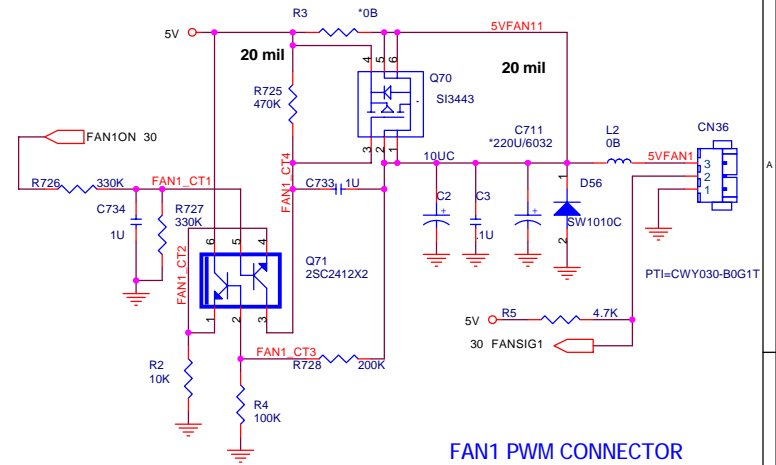


ODD CONNECTOR

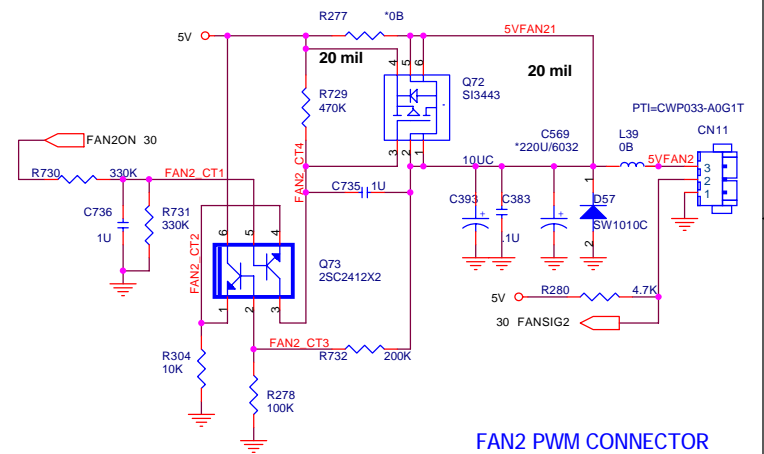


PLACEMENT NOTICE :

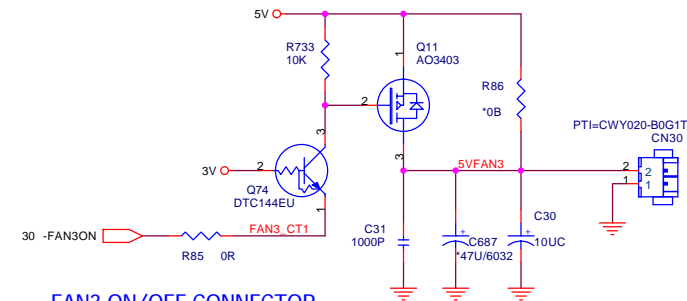
1. PUT THE BYPASS CAP AND INDUCTOR NEAR THE HDD AND ODD CONNECTOR
2. ALL DAMPING RESISTORS SHOULD NEAR ODD AND HDD CONNECTOR RESPECTIVELY
3. ALL PULLUP AND PULLDN SHOULD NEAR THE CONNECTOR
4. ALL IDE TRACE SHOULD KEEP 5:15 ID POSSIBLE AND 5:10 IS MINIMUM REQUIREMENT



FAN1 PWM CONNECTOR



FAN2 PWM CONNECTOR

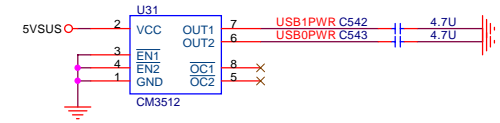
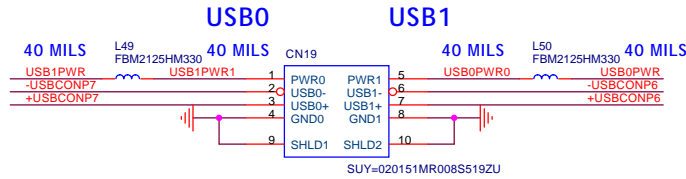
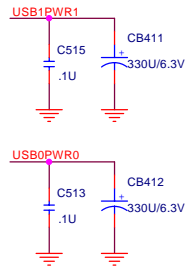
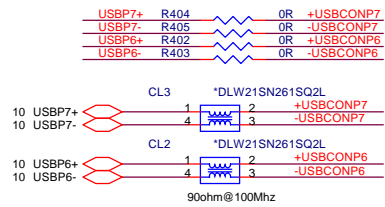


FAN3 ON/OFF CONNECTOR



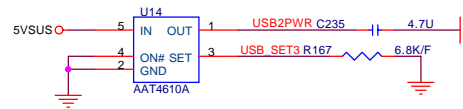
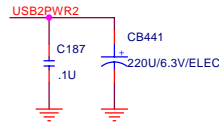
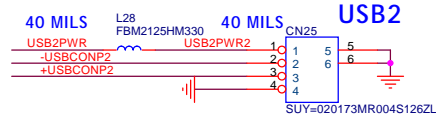
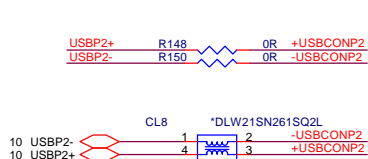
PROJECT : NT2
Quanta Computer Inc.

Size Custom	Document number HDD/CD-ROM/FAN	Rev 3B
Date: Tuesday, January 25, 2005	Sheet 28 of 38	

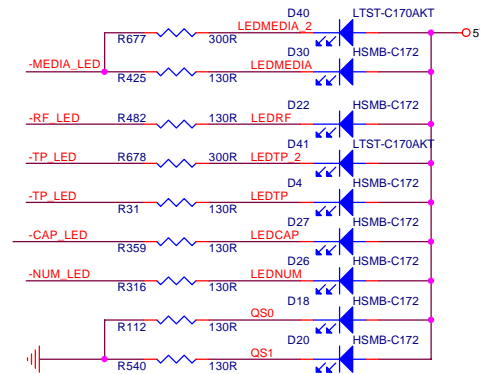
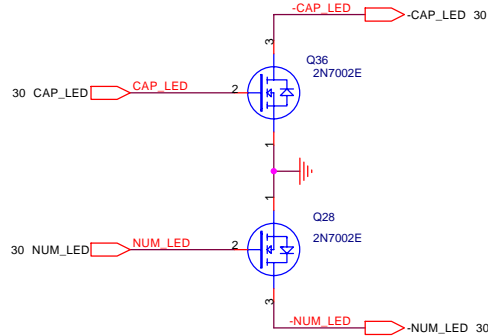
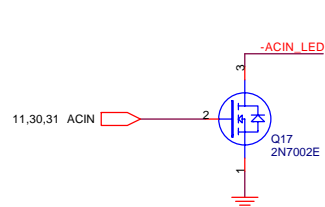
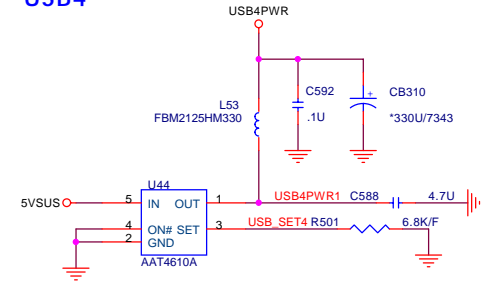


PLACEMENT NOTICE :

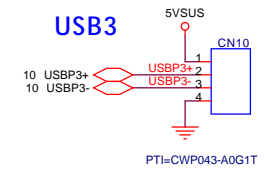
1. ALL USB PORT RELATIVE R/C/L MUST NEAR USB CONNECTOR
2. place the common-mode choke as close as possible to the connector pins
3. max trace length mismatch between usb 2.0 signal pair should be no greater that 150 mils



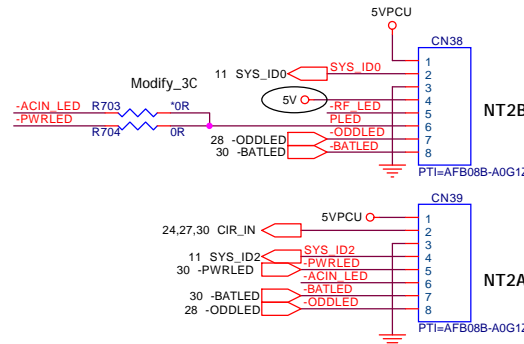
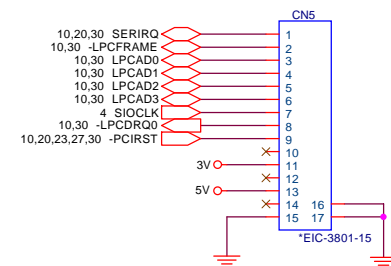
USB4



USB3

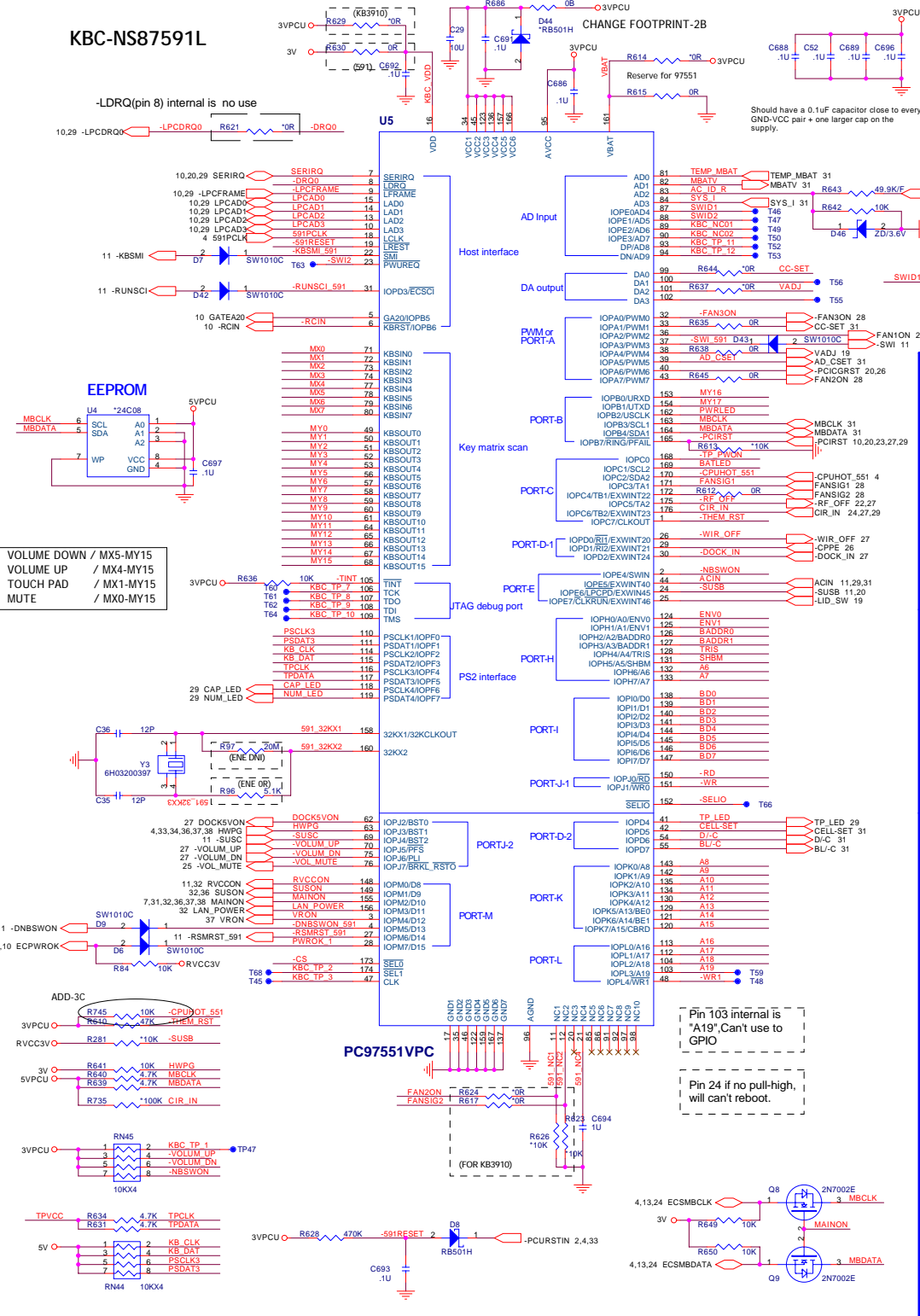


LPC CONN



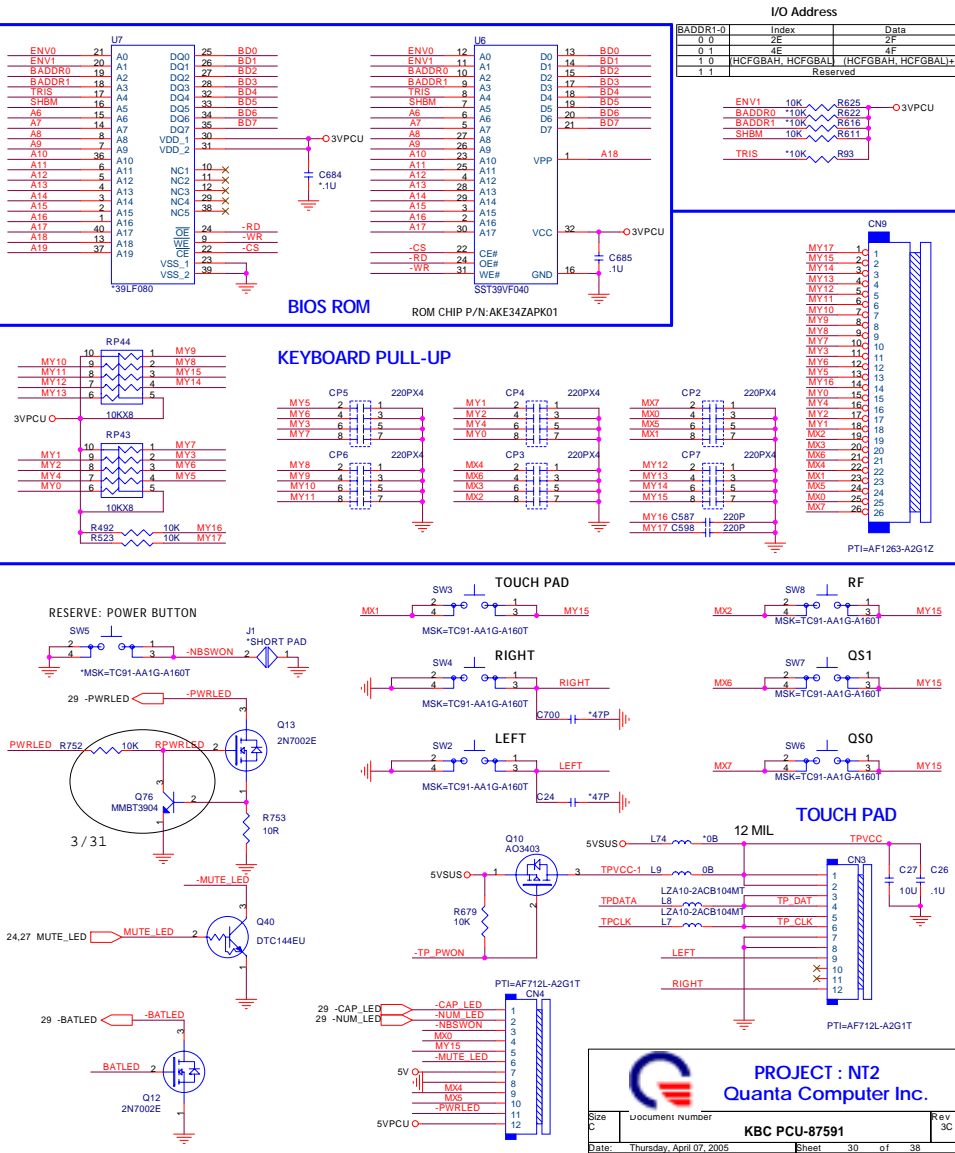
KBC-NS87591L

-LDRQ(pin 8) internal is no use

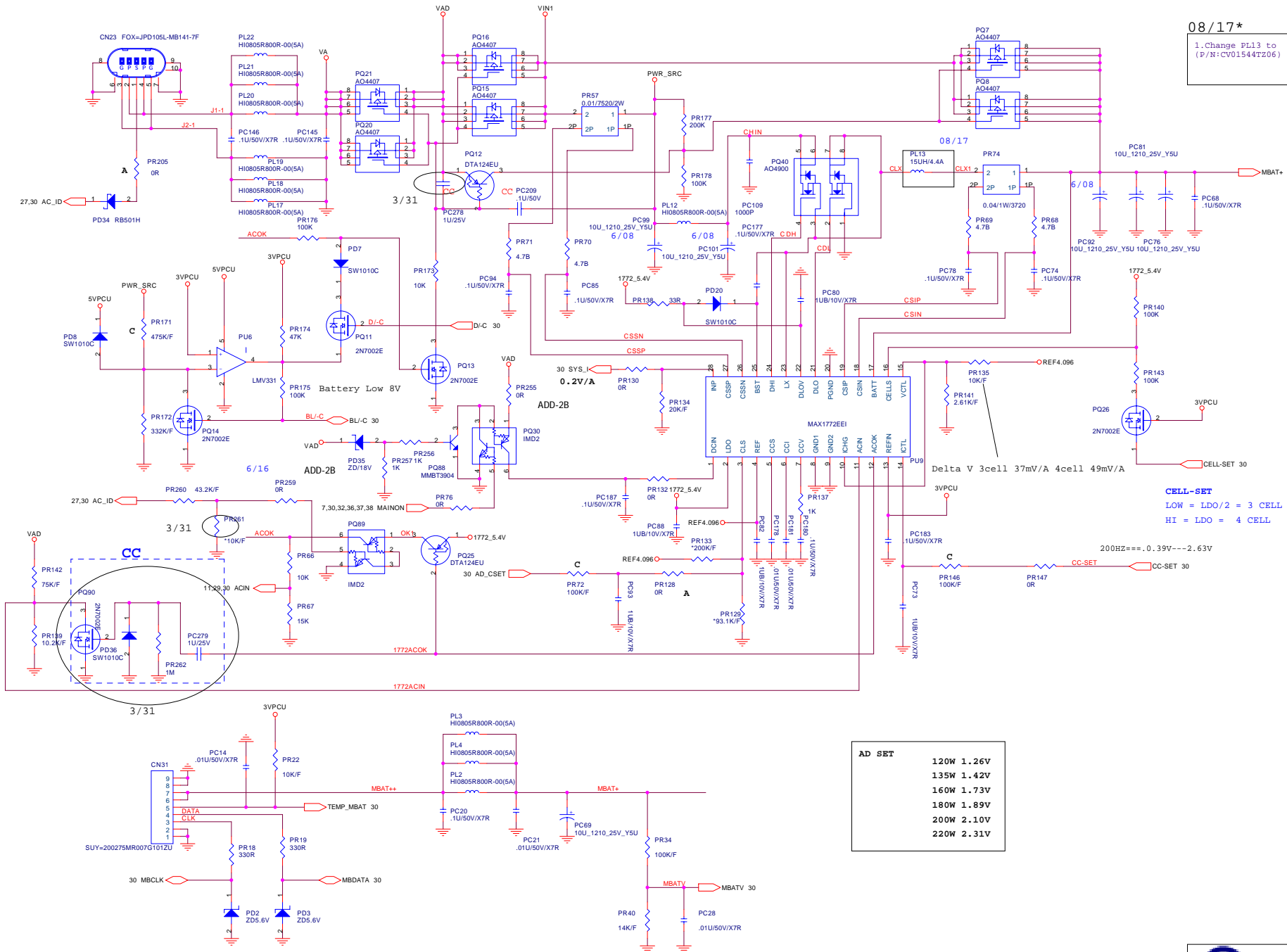


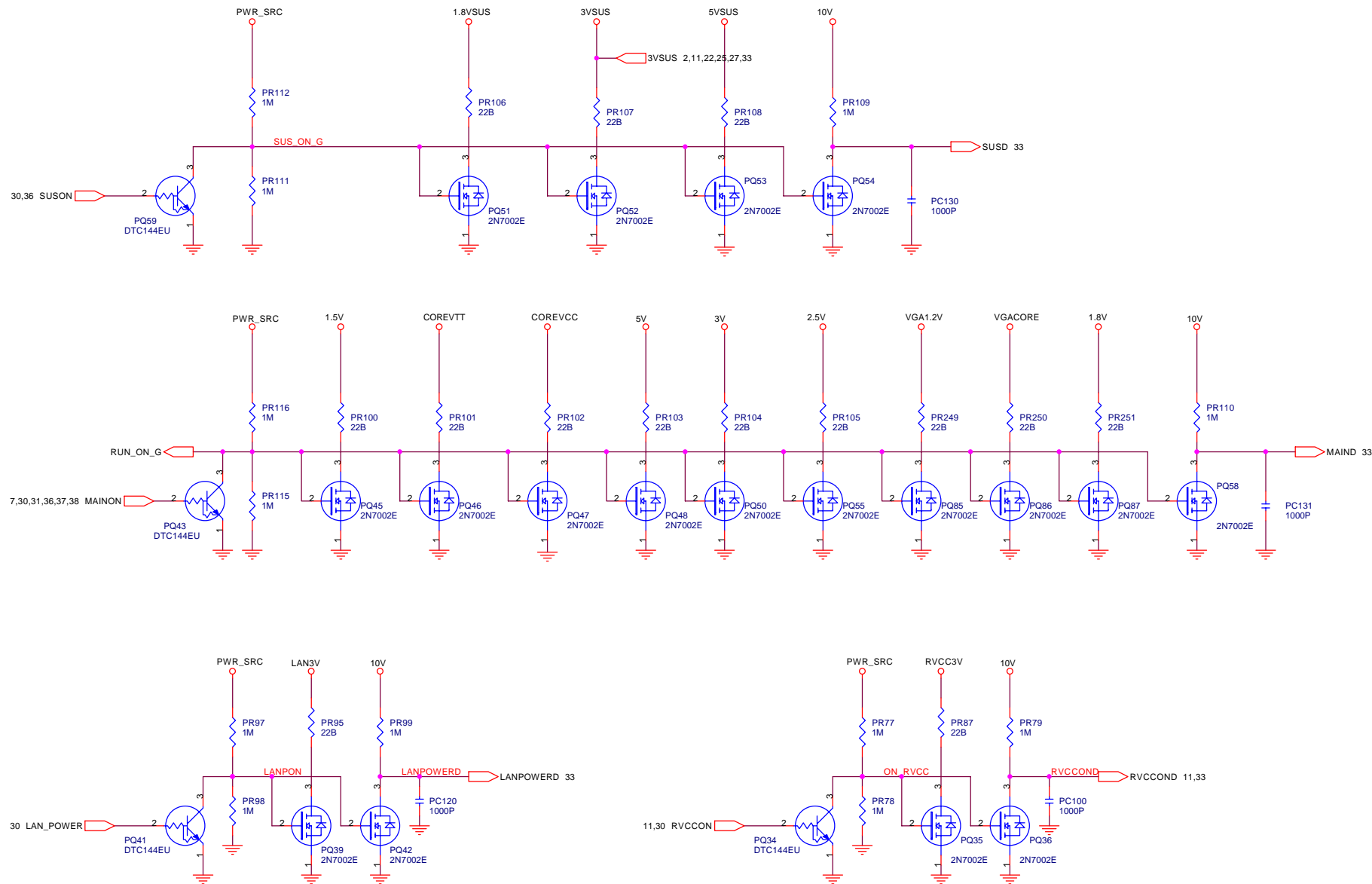
PIN		NS PC87591	ENE KB3910	
11	NC		TEST_TP	High: Clock Test Mode. Low: 32KHz clock in normal running. (Recommend)
12	NC		DPLL_TP	High: Test mode, set K50 [0:15] and K5016 to become internal output. Low: Normal operation. (Recommend)
105	TINT#		ISP_TP	High: Normal operation. (Recommend) Low: Enable ISP mode.
124	ENV0	Internal pull-down to GND. Set the Environment to OBD which is used for debugging the PC87591 firmware while it is mounted on its final production board.	A0	
125	ENV1	External pull-up to 3VPCU by 10k. Set the Environment to OBD which is used for debugging the PC87591 firmware while it is mounted on its final production board.	XIOP_TP	High: Enable the internal pull-up resistor on XIOPS [F:0] pins. Low: Disable the internal pull-up resistor on XIOPS [F:0] pins.
126	BADDR0	Internal pull-down to GND. To set Super I/O configuration Base Address.	A2	
127	BADDR1	Internal pull-down to GND. To set Super I/O configuration Base Address.	A3	
128	TRIS	Internal pull-down to GND. Normal operation.	DMRP_TP	High: Disable Memory Remapping Process. (Recommend) Low: Enable Memory Remapping Process.
131	SHBM	External pull-up to 3VPCU by 10k. Enable shared memory with host BIOS.	EMWB_TP	High: Enable Memory while Boot. (Recommend for shared BIOS application) Low: Disable Memory while Boot.

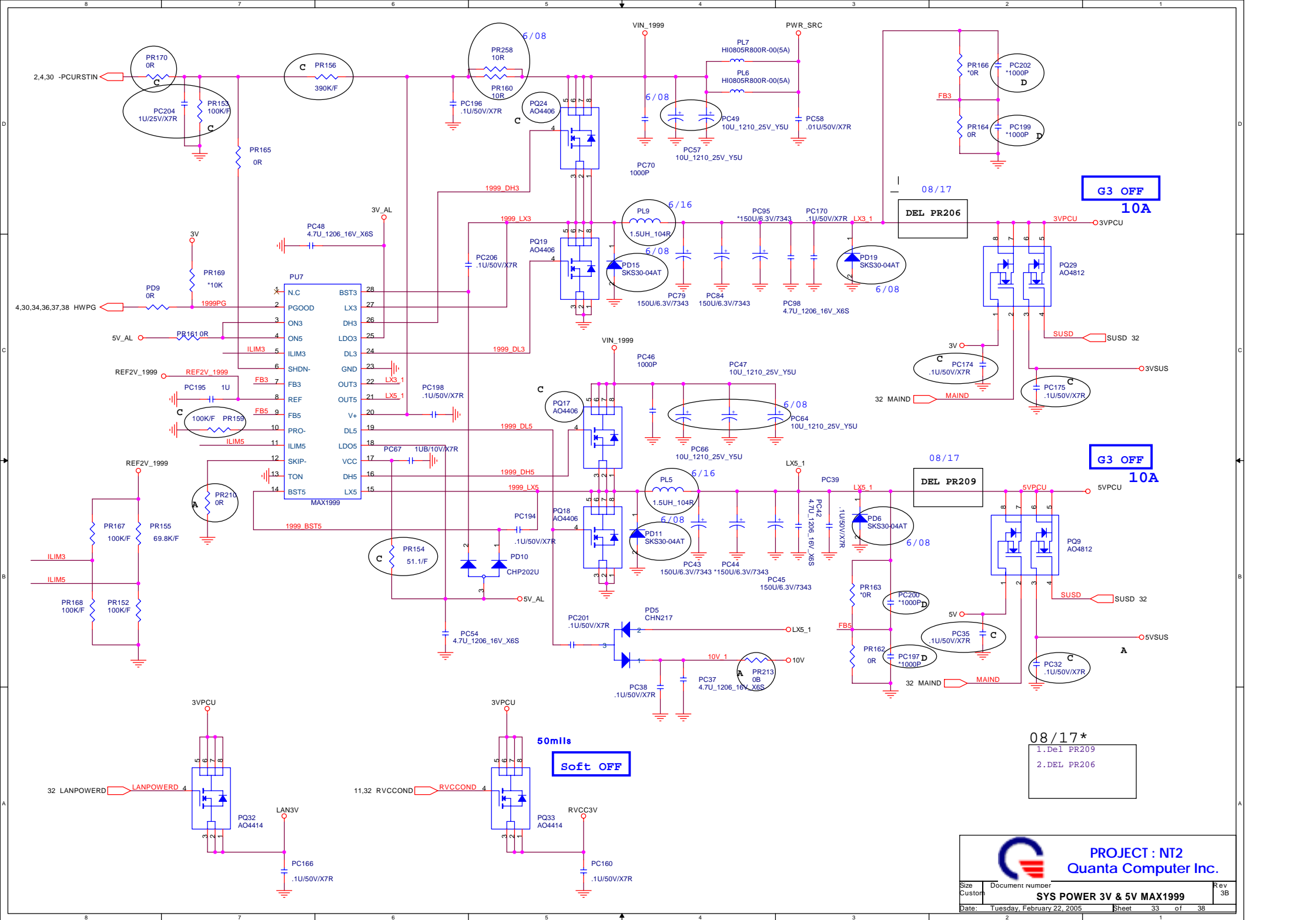
BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	HCFGBAH, HCFGBAL	(HCFGBAH, HCFGBAL)+
1 1	Reserved	



BATTERY CHARGER







MAX1845

